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An Energy-Efficient BJT-Based Temperature-to-Digital Converter with ±0.13°C (3σ) Inaccuracy from -40 to 125°C

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***Abstract*— This paper describes an energy-efficient BJT-based temperature-to-digital converter (TDC) with a state-of-the-art resolution FoM (RFoM) of 5.4pJ·K^2. It consists of a BJT front-end, a capacitively-coupled instrumentation amplifier (CCIA) and a 2nd-order continuous-time (CT) ΔΣADC. The front-end and the CCIA employ bitstream-controlled dynamic element matching (DEM) and chopping to mitigate mismatch and 1/*f* noise without incurring quantization noise fold-back. The sensor achieves ±0.13°C (3σ) inaccuracy from -40 to 125°C and has a supply sensitivity of 8.2mK/V.**

I. Introduction

BJT-based TDCs are widely used, because they only require room-temperature calibration to achieve high accuracy [1-5]. However, they usually employ switched-capacitor (SC) readout architectures, and so their resolution and energy efficiency are limited by kT/C noise. For example, a state-of-the-art TDC achieves a resolution FoM of 7.8pJ·K^2 [4]. Although the design in [5] is more energy-efficient, achieving 3.6pJ·K^2, its output is a duty-cycle modulated signal, which must still be sampled by a high-speed clock and digitized by an external counter. This paper describes a TDC that uses a continuous-time approach. A CCIA is used to boost a PTAT voltage ΔV_{be} (generated by a BJT front-end) before it is digitized by a CT ΔΣADC. As in SC circuits, the CCIA's gain is also determined by a capacitor ratio, resulting in good accuracy and stability. The TDC achieves ±0.13°C (3σ) from -40°C to 125°C, and a state-of-the-art RFoM of 5.4pJ·K^2.

II. Proposed Design

Fig. 1 shows the proposed TDC. A BJT front-end generates PTAT and CTAT voltages ΔV_{be} and V_{be}. The CCIA amplifies ΔV_{be} by a factor $C_{in}/C_{fb} = \alpha/2$. Its output is then applied to a 2nd-order incremental CT ΔΣADC, which implements a charge-balancing scheme, in which $2\cdot\alpha/2\cdot\Delta V_{be}$ is integrated when the bitstream output (bs) is "0" and $-V_{be}$ when bs is "1". This results in a bitstream average $\mu = \alpha\Delta V_{be}/(\alpha\Delta V_{be} + V_{be})$, which is proportional to absolute temperature (PTAT) [6].

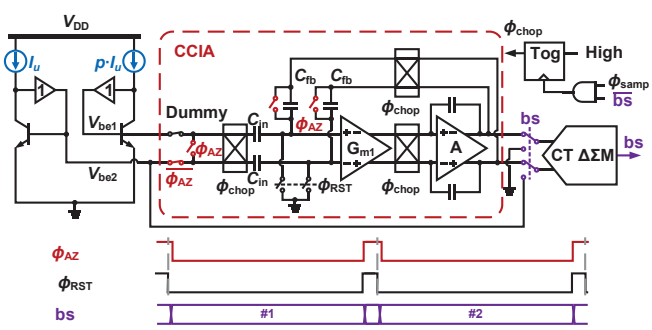

Fig.1 a) Block diagram of the TDC and b) the associated timing.

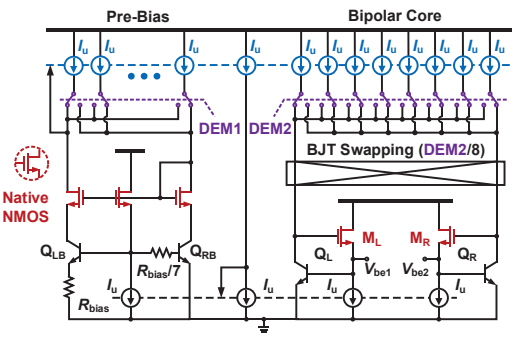

Fig. 2 Simplified schematic of the BJT front-end.

The BJT front-end consists of a bias circuit and a bipolar core (Fig. 2), built around two pairs of identical NPNs (Q_{LB}, Q_{RB}, Q_L and Q_R). Each pair is biased at a collector current ratio of 1:7, with a unit current of 53nA at room temperature. The bias circuit generates a PTAT current that is used by the NPNs of the bipolar core to generate V_{be} and ΔV_{be}. The base currents of the NPNs are provided by source followers M_L and M_R, which also drive the input resistors of the CT ΔΣADC without affecting accuracy. To minimize their mismatch, the current sources of the bipolar core and biasing circuit are dynamically matched. As in [6], this is done in a bitstream-controlled manner to avoid quantization noise fold-back due to intermodulation between the DEM residuals and the modulator's bitstream. To mitigate their mismatch, the NPNs of the sensor core are chopped at the end of every complete cycle of DEM2, avoiding the intermodulation.

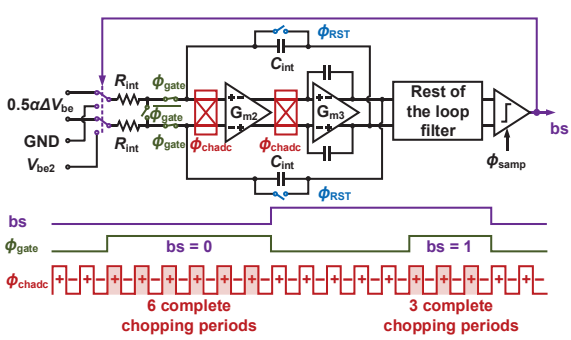

Fig. 3 Block diagram of CT ΔΣADC with the associated timing.

The CCIA consists of a 2-stage Miller-compensated amplifier (Fig. 1). It employs a current-reuse input stage for energy efficiency. Its closed-loop gain is set to $\alpha/2$ (=7), which limits its output swing to ~0.5V over the full temperature range and ensures that its loop-gain is high enough to keep its gain spread below 0.01%. Two CMFB loops (not shown) ensure

adequate robustness to process and temperature variations. The CCIA is also chopped in a bitstream-controlled manner.

At the start of each incremental conversion, the opamp is auto-zeroed by shorting its feedback caps C_{fb} (ϕ_{AZ}, Fig. 1) [7]. This effectively stores the opamp's offset on the input caps C_{in}, resulting in significantly reduced chopping ripple. Therefore, a ripple reduction loop is not required.

At the chopping transitions, the CCIA generates output spikes, which would be a source of error. To avoid this, the input of the 1st integrator of the ΔΣADC is gated as in [8] (Fig. 3). Furthermore, the integrator is chopped at $8f_s$ to suppress its $1/f$ noise and offset. This choice ensures that the chopped offset is always averaged out despite the different lengths of the integration windows corresponding to bs=0 and bs=1 (Fig. 3). To conserve area, the 2nd integrator and feed-forward coefficient are implemented with SC techniques.

III. MEASUREMENT RESUTLS

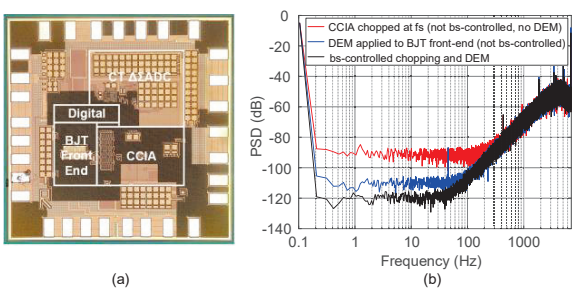

Fig. 4 a) Die micrograph of the TDC, b) PSD of the TDC's bitstream.

Fabricated in a standard 180nm CMOS process, the TDC occupies an active area of 0.35mm^2 (Fig. 4a) and consumes 5.6μA from a 1.6V supply at room temperature. The sinc^2 decimation filter is implemented off-chip. As shown in Fig. 4b, the use of bitstream-controlled chopping and DEM effectively prevents quantization noise fold-back and preserves the noise floor of the BJT front-end.

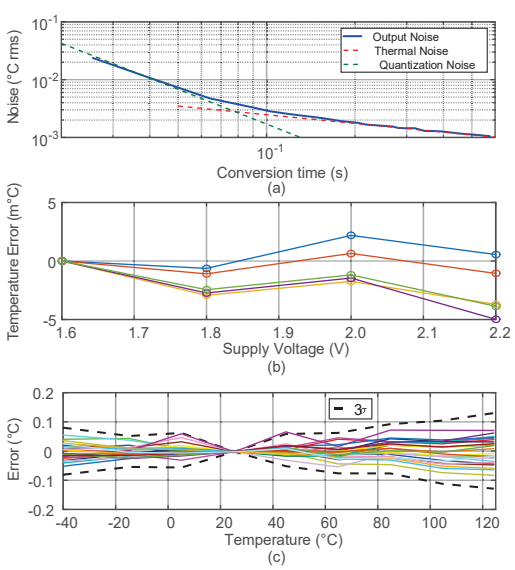

Fig. 5 a) Resolution versus conversion time, b) Temperature error versus supply voltage, and c) Inaccuracy of 25 devices.

When sampled at f_s = 15.625kHz, the TDC achieves a resolution of 1.67mK (rms) in a conversion time of 218ms (Fig. 5a). From 1.6V to 2.2V, its supply sensitivity is 8.2mK/V (Fig. 5b). Measurements were made on 25 devices in ceramic DIL packages. To compensate for V_{be} spread, each sample was calibrated at 25°C. In the same step, the CCIA gain (C_{in}/C_{fb}) of each sample is calibrated with the help of an external voltage. This information is used by the digital backend to perform a PTAT trim on each sample, resulting in an inaccuracy of ±0.25°C (3σ) from -40°C to 125°C. This improves to ±0.13°C (3σ) after a 5th order polynomial is used to remove systematic non-linearity (Fig. 5c). In Table I, the performance of the TDC is summarized and compared with previous BJT-based designs. As can be seen, this work achieves both competitive accuracy and state-of-the-art energy-efficiency.

Table I. Performance summary and comparison with the state-of-the-art.

	JSSC2013 [1]	JSSC2015 [2]	IEEE SJ 2017 [3]	JSSC2017 [4]	This work
Technology	0.16μm	0.16μm	0.18μm	0.16μm	**0.18μm**
Chip area [mm²]	0.54	0.085	0.198	0.16	**0.35**
Supply voltage [V]	1.6	1.4	1	1.5-2	**1.6-2.2**
Supply current [μA]	3.4	4.5	1.1	5	**5.6**
Supply sensitivity (m°C/V)	500	--	--	10	**8.2**
Temperature range	-55°C to 125°C	-40°C to 85°C	25°C to 45°C	-55°C to 125°C	**-40°C to 125°C**
3σ inaccuracy [°C] (Trimming points)	±0.2 (1)	--	±0.2 (1)	±0.06 (1)	**±0.13 (1)**
Conversion time [ms]	5.3	6	500	5	**218**
Resolution [mK]	20	25	10	15	**1.67**
Resolution FoM [pJ·K²] *	11	24	55	7.8	**5.4**

* Resolution FoM = Energy / (Conversion x (Resolution)²)

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