17.4 A Thermal-Diffusivity-Based Temperature Sensor with an Untrimmed Inaccuracy of ±0.2°C (3σ) from –55°C to 125°C

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This paper describes a temperature sensor based on the thermal diffusivity of silicon. Its digital output is insensitive to both process spread and packaging stress and is a near-linear function of absolute temperature. The sensor's accuracy is mainly limited by lithographic resolution, and so benefits from Moore's Law. A sensor fabricated in a 0.18µm CMOS process exhibits an untrimmed device-to-device inaccuracy of ±0.2°C (3σ) from –55°C to 125°C. This is significantly better than that of similar sensors fabricated in a 0.7µm CMOS process [1, 2].

The AC thermal characteristics of silicon are determined by its thermal diffusivity, D. For lightly doped IC-grade silicon, D is insensitive to process spread and has a well-defined temperature dependence [3]. D can be determined by measuring the phase response of an electrothermal filter (ETF), which consists of a heater and a relative temperature sensor located in the same substrate. Fig. 17.4.1 shows a CMOS implementation, in which the heater is an n^+-diffusion resistor and the sensor is a p^+/aluminum thermopile. AC heat diffusing from the heater creates temperature fluctuations at the thermopile, which are low-pass filtered by the substrate's thermal inertia. The phase shift of the thermopile's output (ϕ_{ETF}), with respect to a harmonic heater drive signal (f_{drive}), is determined by D and by s, the spacing between the heater and the thermopile. For a constant f_{drive}, ϕ_{ETF} is a near-linear function of absolute temperature [1].

The spread of ϕ_{ETF} is mainly determined by spread in the position of the diffusion/aluminum contacts, since this defines the effective value of s (Fig. 17.4.1). This, in turn, is determined by the lithographic accuracy of the process. In a 0.7µm CMOS process, with s ~ 23µm, this resulted in a temperature inaccuracy of about ±0.7°C (3σ) [2]. In this work, greater accuracy was achieved by improving the interface electronics and by leveraging the more accurate lithography of a 0.18µm process.

As shown in Fig. 17.4.2, ϕ_{ETF} is digitized by a 1st-order phase-domain ΔΣ modulator (PDΔΣM). The ETF's output signal, V_{ETF}, is first converted to a current by a g_m-stage, and then multiplied by a copy of f_{drive} with a relative phase shift of ϕ_{fb}. The multiplier implements a phase-differencing node, since the DC component of the resulting current, I_{demod}, is proportional to $\cos(\phi_{ETF}-\phi_{fb})$. This current is then applied to the loop filter: an active integrator. Based on its output, a comparator selects ϕ_{fb} from one of two digitally generated phase references (ϕ_0 and ϕ_1), which straddle the temperature range of interest.

When driven by a 42kHz 2.5mW square wave, the amplitude of the ETF's output is rather small (~400µV_{pp}). Since the thermopile's resistance (R_{tp} = 20kΩ) produces thermal noise, measurement bandwidth must be traded off against temperature-sensing resolution. The PDΔΣM's sinc decimation filter can be used to define a conversion rate of 0.16Hz, which corresponds to a temperature sensing resolution of 0.02°C_{rms}. At a sampling frequency of f_{drive}/4, this bandwidth results in an OSR of 32768, which is high enough to ensure that the modulator's resolution is thermal-noise limited.

The g_m-stage consists of a gain-boosted folded cascode OTA (Fig. 17.4.3). Its transconductance was set to 600µS, which ensures that the thermopile is the dominant source of thermal noise. Gain boosting is used to obtain high output impedance, which, together with the gain of the active integrator, minimizes integrator leakage. The phase-differencing node is implemented by a chopper CH1, located at the virtual ground of a gain-boosting differential amplifier [2]. The phase shift of the circuitry before the demodulator spreads over PVT, and should be negligible compared to ϕ_{ETF}. To this end, the pole at the folding node was located at ≥100MHz. For this circuit, this translates into a phase spread (over corners) of less than 4m° at f_{drive}, corresponding to a temperature error below 0.02°C.

The offset of the g_m-stage and the DC component of V_{ETF} are modulated to f_{drive} by CH1. These signals are ≥25x larger than the AC component of V_{ETF} and result in large ripple at the integrator output (>1V_{pp}), which consumes significant headroom (since V_{dd} = 1.8V). Therefore, the g_m-stage is auto-zeroed at the start of each conversion via an auxiliary differential pair (Fig. 17.4.3). To avoid sampling the AC component of the ETF's output, the ETF is driven at 16×f_{drive} during this phase. Since the ETF is a thermal LPF, this greatly suppresses the AC component without affecting the DC component, which ensures that the residual ripple at the integrator's output is at the noise level.

The active integrator is built around a two-stage opamp with a DC gain of 80dB. With C_{int} = 24pF, the voltage swing at its output is about 300m$V_{pp\text{-}diff}$. The opamp's offset interacts with the g_m-stage's finite output impedance to create an offset current, which corresponds to a temperature error of about 0.5°C (worst-case). Offset currents of similar magnitude are also caused by the charge injection of CH1. Both these offset currents are chopped once per conversion by the low-frequency chopper CH2. To maintain the correct signal polarity at the output of the phase detector, f_{drive} is synchronously inverted. The resulting low-frequency ripple is filtered out by the decimation filter [2].

The ETF and a PDΔΣM were realized on a 0.18µm CMOS chip with an active area of 0.18 mm^2 (Fig. 17.4.7). The PDΔΣM consumes 500µW (5x less than in [1, 2]), and P_{heat} was set to 2.5mW. The required driving signals (f_{drive}, f_s, etc.) were generated from a 16MHz crystal oscillator reference clock; the reference phase shifts ϕ_0 and ϕ_1 were set to -67.5° and -11.25°, respectively. Measurements on the PDΔΣM alone show that its phase spread corresponds to a total error of ±0.1°C (3σ).

The measured bitstream average (ϕ_{ETF}) as a function of temperature is shown in Fig. 17.4.4, and Fig. 17.4.5 shows an FFT of the bitstream. A batch of 16 devices was packaged in ceramic DIL packages. As shown in Fig. 17.4.6, their untrimmed inaccuracy is ±0.2°C (3σ) over the military temperature range (-55°C – 125°C). These results are comparable to state-of-the-art batch calibrated temperature sensors based on bipolar transistors [4]. Measurements made on 16 devices from a second wafer in plastic TSSOP packages resulted in the same characteristic, but with a somewhat greater spread of ±0.3°C (3σ). These results demonstrate that ETFs are insensitive to both process spread and to the random mechanical stress caused by plastic packaging.

The improved lithographic resolution of a 0.18µm CMOS process can be used to reduce the heater power required for a certain temperature-sensing resolution. To test this, a second ETF was realized with 1.7x more thermocouples than the ETF in [2]. With s ~ 11µm, it was also somewhat smaller. For a fair comparison, the thermopile's resistance R_{tp}, and hence its noise, was kept the same. The measured temperature spread increased to ±0.4°C (3σ), but to obtain the same resolution as in [2], i.e. 0.03°C_{rms} into a 0.16Hz bandwidth, 3x less heating power (833µW) was required.

References:

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[2] S.M. Kashmiri, S. Xia, K.A.A. Makinwa, "A temperature-to-digital converter based on an optimized electrothermal filter", *IEEE Journal of Solid State Circuits*, pp. 2026 - 2035, Jul. 2009.
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[4] A.L. Aita, M.A.P. Pertijs, K.A.A. Makinwa and J.H. Huijsing, "A CMOS smart temperature sensor with a batch-calibrated inaccuracy of ±0.25°C (3σ) from -70°C to 130°C", *IEEE ISSCC Dig. Tech. Papers*, pp. 342-343, Feb. 2009.

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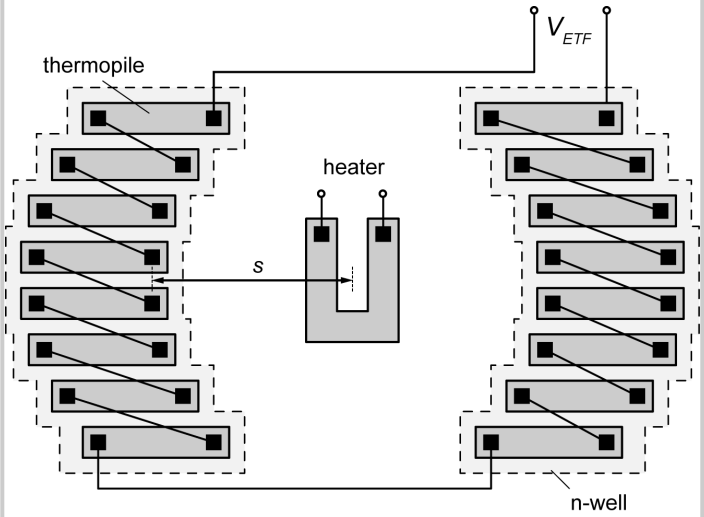

Figure 17.4.1: Schematic layout of an Electrothermal Filter (ETF).

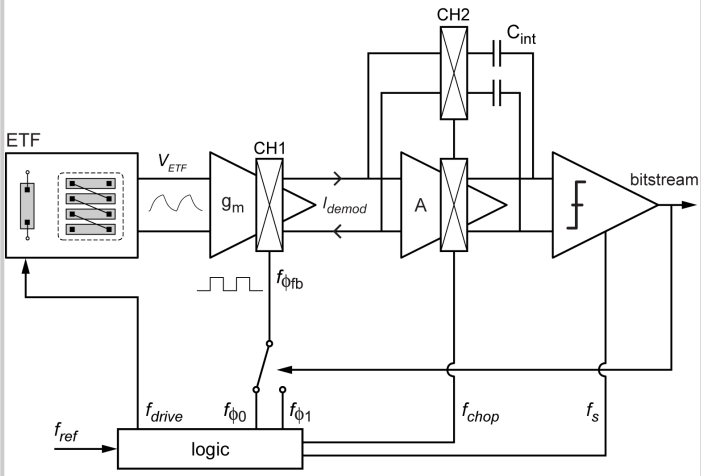

Figure 17.4.2: System diagram of an ETF read out by a phase-domain ΔΣ modulator (PDΔΣM).

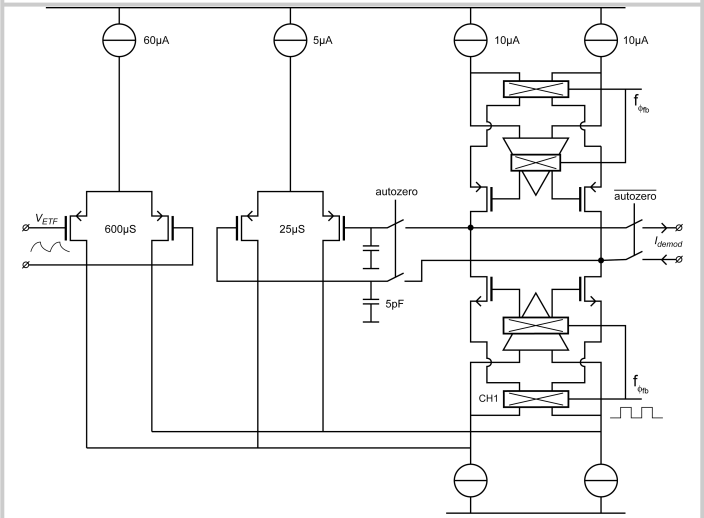

Figure 17.4.3: Schematic of the gain-boosted auto-zeroed g_m-stage. The ETF's output voltage V_{ETF} is converted to a current and then synchronously demodulated by $f_{\phi fb}$.

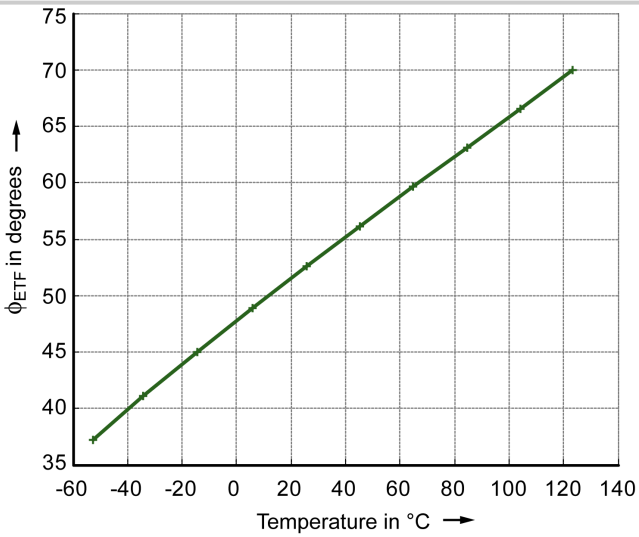

Figure 17.4.4: Measured digital representation of ϕ_{ETF} as a function of temperature.

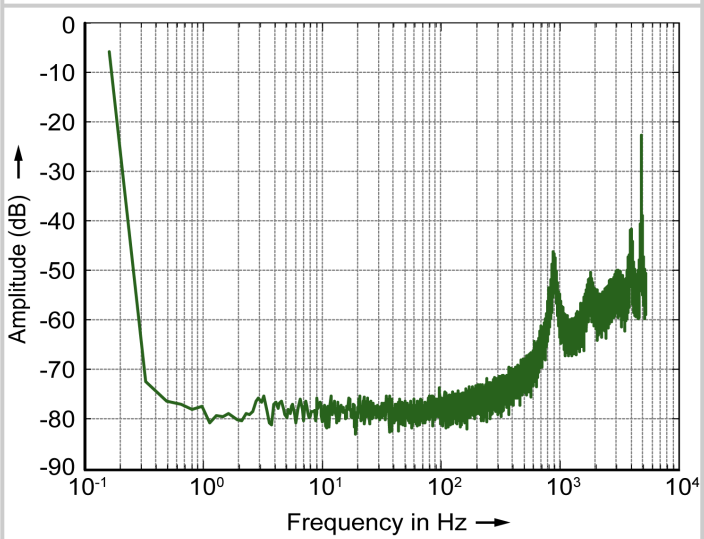

Figure 17.4.5: FFT of the measured bitstream; linear average of 10 65536-point FFTs, Hanning-windowed. The low-frequency chopper was switched off.

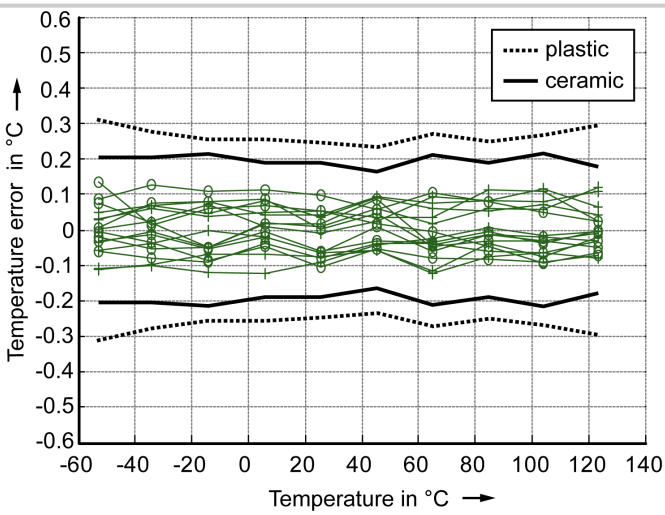

Figure 17.4.6: Measured untrimmed temperature error for 16 devices from a single batch. The black lines indicate the ±3σ limits. The dashed lines indicate the ±3σ limits for 16 devices packaged in plastic TSSOP packages.

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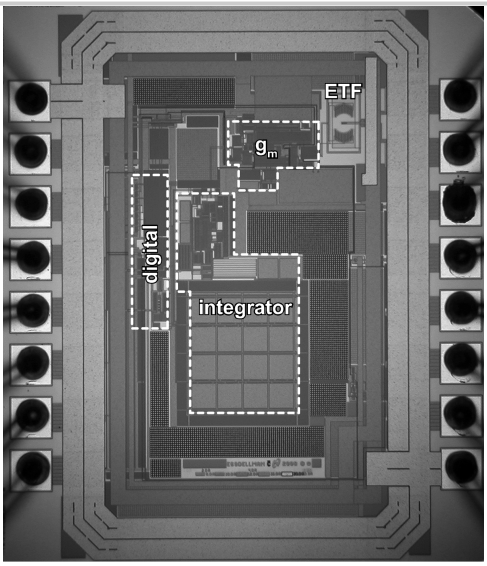

Figure 17.4.7: Chip photo.

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