A CMOS Temperature-to-Frequency Converter With an Inaccuracy of Less Than $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) From $-40\,^{\circ}\mathrm{C}$ to $105\,^{\circ}\mathrm{C}$

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***Abstract*—This paper describes a temperature-to-frequency converter (TFC) implemented in a standard CMOS process. Its output frequency is determined by the phase-shift of an electrothermal filter, which consists of a heater and a temperature sensor realized in the substrate of a standard CMOS chip. The filter's phase-shift is determined by the geometry of the thermal path between the heater and the sensor, and by the temperature-dependent rate at which heat diffuses through the substrate. The resulting temperature-dependent phase-shift is quite well-defined, since filter geometry is defined by lithography, while the thermal diffusivity of the high-purity lightly-doped silicon substrate is essentially constant. The filter was used as the frequency-determining component of a frequency-locked loop (FLL), whose output frequency is then a well-defined function of temperature. Using this approach, a TFC with an inaccuracy of $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) over the industrial temperature range ($-40\,^{\circ}\mathrm{C}$ to $105\,^{\circ}\mathrm{C}$) has been realized in a standard 0.7-μm CMOS process.**

***Index Terms*—Chopper modulation, electrothermal integrated circuit, frequency-locked-loop (FLL), temperature sensors.**

I. Introduction

TODAY, most integrated temperature sensors make use of the temperature dependence of bipolar transistors [1]–[3]. Due to process spread, such sensors typically exhibit an inaccuracy of only a few degrees Celsius. This can be greatly reduced, to less than $\pm 0.1\,^{\circ}\mathrm{C}$ (3σ) over the military temperature range [4], by calibrating and trimming individual sensors. However, this is at the expense of increased manufacturing costs. The use of batch calibration, in which calibration data from a few samples is used to trim an entire batch, is significantly cheaper, but this results in increased inaccuracy [4], [5].

An alternative method of realizing an integrated temperature sensor is by measuring the *temperature-dependent* rate at which heat diffuses through silicon [6]–[8]. This can be done by measuring the temperature-dependent phase-shift of an electrothermal filter. In most IC processes, such a filter can be readily implemented by integrating a heating element and a temperature sensor on the same silicon substrate [6], [9], [10]. Electrical power dissipated in the heater induces temperature differences in the substrate, which are then transformed back to the electrical domain by the temperature sensor. Due to the substrate's thermal inertia, this structure behaves like a low-pass filter, whose phase shift is determined by the geometry of the thermal path between heater and sensor, and by the temperature-dependent thermal diffusion constant of the substrate. Variations in the former can be mitigated by making the filter's dimensions sufficiently large, while the latter is essentially constant over the industrial temperature range, at least for the high-purity low-doped (resistivity greater than 6 Ωcm) substrates typically used in most modern IC processes [11], [12]. As a result, the phase shift of a properly designed electrothermal filter will be a well-defined function of temperature.

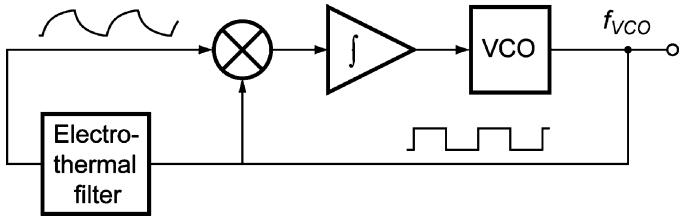

Fig. 1. Block diagram of an electrothermal frequency-locked-loop (FLL).

One way of determining the temperature-dependent phase-shift of an electrothermal filter is by using the filter as the frequency-determining component of a feedback or relaxation oscillator [6]–[8], [13]. The frequency of the resulting electrothermal oscillator will then be a well-defined function of temperature, i.e., the oscillator is a temperature-to-frequency converter (TFC). Compared to an electrical oscillator, however, the power dissipation and jitter of such an oscillator is rather poor. This is because silicon is a good thermal conductor, and as such electrothermal filters are rather inefficient, with milliwatts of heating power typically creating temperature differences of only a few tenths of a degree. Their output is then rather small (at the millivolt-level), resulting in a poor SNR, which, in turn, leads to an oscillator with poor jitter [7]. Although improved efficiency can be obtained by realizing the filter on an isolating diaphragm [14], this requires a micromachining step that is not available in standard IC processes.

Recently, an improved temperature-to-frequency converter (TFC) was presented in which the phase-shift of an electrothermal filter determines the frequency of an electrical voltage-controlled oscillator (VCO) [15]. As shown in Fig. 1, the TFC is a frequency-locked-loop (FLL) consisting of a VCO, a synchronous phase-detector and an electrothermal filter. The loop is arranged such that its steady-state output frequency corresponds to a *fixed* phase-shift in the electrothermal filter. The filter is driven by the square-wave output of the VCO, and its phase-shifted output is synchronously demodulated

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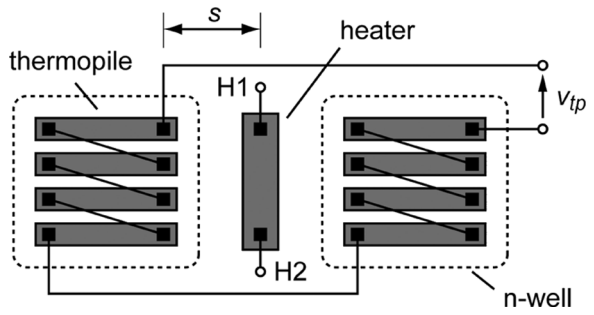

Fig. 2. Schematic layout of a CMOS electrothermal filter.

by multiplying it with the same square-wave. The output of the multiplier is then integrated and used to tune the VCO's frequency. The loop settles when the DC output of the multiplier is zero, which corresponds to a constant phase-shift in the electrothermal filter. Since the multiplier's DC output is zero at steady-state, the resulting VCO frequency is insensitive to variations in the *amplitude* of the filter's output. Compared to electrothermal relaxation or feedback oscillators, the main advantage of this topology is that the multiplier and integrator act like a narrowband tracking filter, significantly limiting the loop's noise bandwidth and, therefore, reducing jitter and increasing temperature-sensing resolution. Using this approach, the TFC described in [15] achieved a resolution of less than 0.2 °C, and an inaccuracy of less than ±2 °C (3σ) over the temperature range from −50 °C to 125 °C.

Apart from an integrated electrothermal filter and a low-offset preamplifier, however, the TFC of [15] was implemented mainly with discrete components. In this paper, an improved TFC with a higher degree of integration and increased accuracy is presented. In Section II, a brief introduction to the properties of electrothermal filters is given. This is followed, in Section III, by a discussion of the considerations governing the design of an electrothermal filter for temperature sensing. The implementation of the TFC's interface electronics is described in Section IV. Experimental results are presented and discussed in Section V. The paper ends with a discussion of the measurement results and conclusions.

II. Characteristics of Electrothermal Filters

The layout of an electrothermal filter implemented in standard CMOS technology is shown in Fig. 2. The heater is an n^+ diffusion resistor, while the temperature sensor is a thermopile realized from p^+ diffusion/aluminum thermocouples. Compared to other integrated temperature sensors such as transistors or resistors, thermocouples are free of offset and $1/f$ noise, which makes them well suited for measuring small on-chip temperature variations. Of the various thermocouples available in a standard CMOS process, the p^+ diffusion/aluminum thermocouple was chosen because of its relatively high sensitivity (∼0.5 mV/K), and because it is realized in an n-well, which can then be used as an electrostatic shield [16], [17]. To further increase the thermal efficiency of the filter, the thermocouples are located on both sides of the rectangular heater.

Electrical power dissipated in the heater creates localized temperature differences in the substrate, which are then sensed

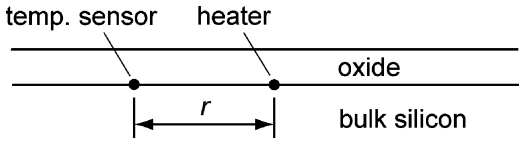

Fig. 3. Idealized cross section of an electrothermal filter consisting of a point heater and a point temperature sensor.

by the thermopile. In order to predict the filter's performance, a model of its frequency response is required. Since exact analytical models of even simple filter geometries are rather complex [9], [10], [18], the heater is modeled as a collection of point heat sources, whose contributions to the thermopile output can then be obtained with the help of relatively simple equations.

An electrothermal filter consisting of a point heat source and a point temperature sensor, both located at the surface of a silicon chip, is shown in Fig. 3. The layer of oxide covering the filter may be regarded as an ideal insulator, since its thermal conductivity is nearly two orders of magnitude less than that of bulk silicon. The transfer function Z_P relating the temperature *rise* T at the sensor to the heater power dissipation P is then given by [18]

$$Z_P(\omega,r)=\frac{T(\omega,r)}{P(\omega)}=\frac{1}{2\pi kr}\exp\left(-r\sqrt{\frac{\omega}{2D}}\right)\exp\left(-jr\sqrt{\frac{\omega}{2D}}\right) \quad (1)$$

where r is the distance between heater and sensor, $D=k/\sigma c$ is the thermal diffusion constant of the substrate (0.88 cm^2/s at 300 K for high-purity silicon [12]), k is its thermal conductivity, σ is its density, and c is its specific heat capacity. The transfer function Z_P has units of K/W and is therefore a thermal impedance. Its magnitude and phase are

$$\text{Magnitude}: \ |Z_P(\omega,r)|=\frac{1}{2\pi kr}\exp\left(-r\sqrt{\frac{\omega}{2D}}\right) \quad (2)$$

$$\text{Phase}: \qquad \arg\left(Z_P(\omega,r)\right)=\left(-r\sqrt{\frac{\omega}{2D}}\right). \quad (3)$$

From these equations it may be seen that this electrothermal filter does indeed have a low-pass characteristic (Fig. 4).

In the FLL shown in Fig. 1, the electrothermal filter is driven by a square-wave. To a first approximation, the higher order harmonics will be attenuated at the filter output and can be neglected. At steady-state, i.e., when the DC output of the demodulator is zero, the phase-shift of the first harmonic will then be exactly -90°, and so from (3), the corresponding frequency f_{zero} is given by

$$f_{\text{zero}}\sim\frac{\pi D}{4r^2}. \quad (4)$$

That is, the VCO's output frequency is a function of the filter's geometry and of the thermal diffusion constant of the substrate. The actual value of f_{zero}, taking into account the presence of higher order harmonics and solving numerically, is only about 3% lower than that predicted by (4).

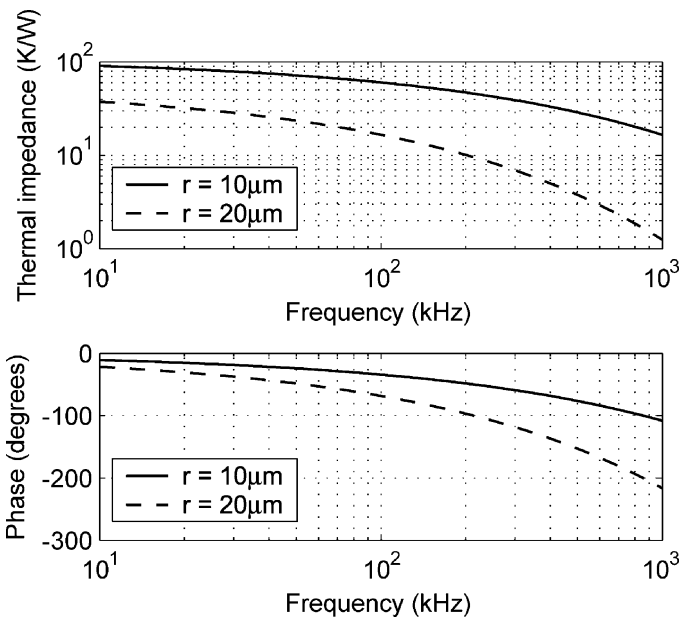

Fig. 4. Thermal impedance at a distance r away from a point heater.

III. Filter Design Considerations

The most important consideration in the design of an electrothermal filter for temperature sensing is the effect of lithographic inaccuracy or process spread. From (4), this will give rise to spread in the VCO frequency, and hence in the estimated temperature. The temperature dependence of D over the industrial temperature range can be approximated to within a few percent by a power law, i.e., $D \propto T^{-n}$ where T is absolute temperature and $n \sim 1.8$ (based on the recommended values of D for high-purity undoped silicon over the temperature range 250 K to 400 K [12]). The steady-state value of $f_{\rm zero}$ may then be expressed as

$$f_{\rm zero} \propto \frac{1}{T^n r^2}. \tag{5}$$

Regarding (5) as an implicit equation expressing T in terms of r and then differentiating, we obtain

$$\frac{dT}{T} = \left(-\frac{2}{n}\right)\frac{dr}{r}. \tag{6}$$

This indicates that the spread in the estimated temperature can be minimized by making the distance r sufficiently large. From (3), however, as r increases the filter's output will drop rapidly, and so there is a trade-off between accuracy and resolution. In the chosen 0.7-μm CMOS process, the lithographic inaccuracy is assumed to be less than 70 nm, i.e., 10% of the minimum line width. If the maximum desired inaccuracy at room temperature is 0.5 °C, then from (6), the minimum value of r should be 49 μm. This suggests that the thermopile/heater spacing s of the filter layout shown in Fig. 2 should be of roughly the same order of magnitude. However, the filter's differential layout may be expected to reduce the inaccuracy by at least a factor of two. Furthermore, the actual filter may be regarded as a superposition of many point source filters, which will further reduce the effect of random lithographic errors. For these reasons, it was decided to implement two electrothermal filters, one with the thermopile/heater spacing $s = 20$ μm (ETF1) and the other with $s = 10$ μm (ETF2), to investigate the trade-off between accuracy and signal level.

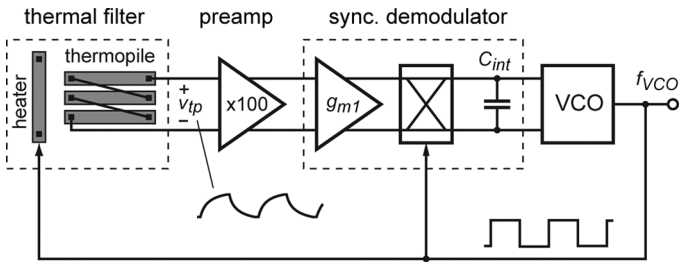

Fig. 5. Practical implementation of an electrothermal FLL.

Although the signal level at the filter output can be increased simply by increasing heater power dissipation, this will be limited by self-heating considerations. Given that a typical packaged chip will have a thermal resistance to ambient of some 100°C/W, which can be expected to spread by about 20% from device to device, a heater power dissipation of 25 mW will, itself, cause the resulting temperature rise to spread by 0.5 °C. With this in mind, the heater consists of a near minimum-width n^+ diffusion resistor with a nominal resistance of 1.25 kΩ, which then dissipates some 10 mW when driven by a 5 V square-wave. The thermopile consists of 10 thermocouples, spaced at a near-minimum pitch, located on each side of the rectangular heater (Fig. 2).

At a temperature of 300 K and a heater power dissipation of 10 mW, Matlab simulations based on the point source model predict that for ETF1, $f_{\rm zero}$ is about 126 kHz, while the output amplitude is about 0.7 mV. For ETF2, the output amplitude increases, to 1.0 mV, and $f_{\rm zero}$ is about 390 kHz.

IV. Circuit Implementation

Being only at the millivolt level, the thermopile output must be amplified before it can be measured or processed further. This consideration leads to the inclusion of a preamplifier in a practical realization of an electrothermal FLL. This is shown in Fig. 5, and consists of a preamplifier with a gain of 100 whose output is then applied to a synchronous demodulator consisting of transconductor g_{m1}, a chopper, and an external capacitor $C_{\rm int}$.

At $f_{\rm zero}$, the preamplifier's phase-shift, which spreads over process and temperature, should be negligible compared to the -90° phase-shift of the electrothermal filter. For the expected values of $f_{\rm zero}$, this corresponds to a preamplifier bandwidth of several tens of megahertz. To achieve this in a power efficient manner, the preamplifier was implemented using an open-loop, four-stage topology. Each stage consists of a pMOS transconductor and a near minimum-size pMOS diode load (Fig. 6). The matching of these elements ensures that the preamplifier's gain and bandwidth are sufficiently well defined over process and temperature.

To prevent the preamplifier's output-referred offset from saturating the synchronous demodulator, a DC servo loop consisting of transconductor g_{m2} (a telescopic OTA with a resistor-degenerated input pair), capacitor $C_{\rm dc}$ and transconductor g_{m3} (a simple differential pair) was also implemented. This reduces the

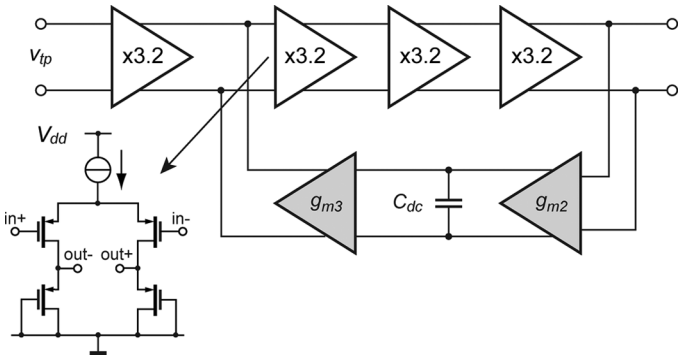

Fig. 6. Block diagram of the thermopile preamplifier.

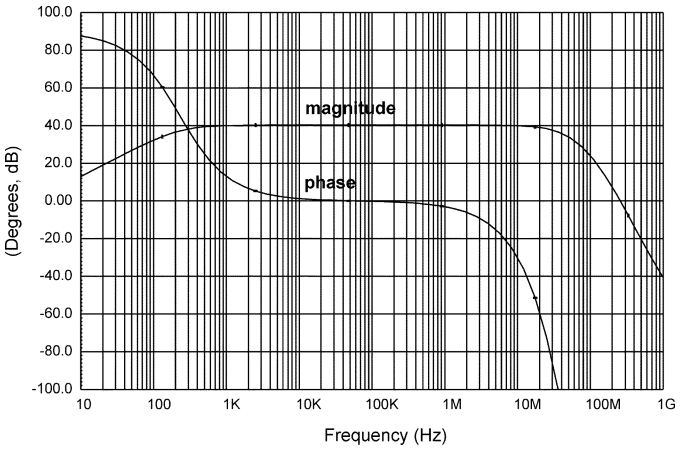

Fig. 7. Frequency response of the thermopile preamplifier.

output-referred offset to the level of the offset of g_{m2}, i.e., typically several millivolts, but causes the preamplifier to have an overall high-pass characteristic. To avoid introducing significant electrical phase-shift at $f_{\rm zero}$, the corresponding corner frequency must be only a few hundred Hertz. The required value for $C_{\rm dc}$ is then rather large, in the order of 100 nF, and was, therefore, implemented off-chip. At 300 K, the simulated frequency response of the preamplifier is shown in Fig. 7, with $C_{\rm dc} = 100$ nF. The preamplifier then has a low-frequency corner frequency of about 250 Hz, and a bandwidth of about 32 MHz.

In addition to the amplified thermopile output, the offset of both g_{m1} and g_{m2} will be present at the input of the demodulator. This is not a problem, since it will be modulated to $f_{\rm VCO}$ by the chopper and then filtered out by the integrator. The chopper's charge injection mismatch, however, will result in a residual offset *current* into $C_{\rm int}$, which will introduce a significant equivalent phase error. To reduce this, the thermal filter, preamp and g_{m1} are chopped *again* at the lower frequency of $f_{\rm VCO}/128$. As shown in Fig. 8, this was done by adding an extra off-chip chopper before $C_{\rm int}$ and modifying the heater drive logic so that the polarity of the generated *heat* is periodically inverted.

A further source of error is cross-talk (via parasitic capacitances or the substrate) between the voltages applied to the heater and the thermopile output. The resulting spikes (Fig. 9) are in phase with the heater drive, and will give rise to a DC error signal at the output of the demodulator. To eliminate this source of error, the polarity of the heater drive is periodically inverted (at $f_{\rm VCO}/64$) by the heater drive logic. While this does not alter the generated heat, it does invert the spike polarity periodically (Fig. 9), turning it into an AC signal which will be filtered out by the integrator.

V. Measurement Results

The preamp, synchronous demodulator and two electrothermal filters were realized on a 2.3 mm^2 chip (Fig. 10) fabricated in a standard 0.7-μm CMOS process. The on-chip electronics (excluding the heaters) dissipates 2.5 mW from a 5 V supply. The rest of the TFC, i.e., the VCO and the heater drive logic, was implemented off-chip. Also, an off-chip instrumentation amplifier (with a gain of 10) was used to convert the differential output of the demodulator into the single-ended control signal required by the VCO.

Measurements were made on nine samples from one batch. Each sample was mounted in a ceramic DIL-16 package, and placed in an oven. The temperature of the samples was measured by a platinum thermometer, which was calibrated to within 20 mK at the Dutch Institute of Metrology. For the measurements, $C_{\rm int} = 1$ μF, which corresponds to a FLL bandwidth of 0.5 Hz (as estimated from the system's step response).

Measurements obtained with ETF1 operated at a heater power dissipation of 2.5 mW are shown in Fig. 11. It may be seen that $f_{\rm zero}$ has the expected $1/T^n$ dependence, where T is the absolute temperature in Kelvin, and $n = 1.7$. This value of n for the lightly-doped substrate is in good agreement with the value of 1.8 derived for high-purity undoped silicon (Section III). As shown in Fig. 12, the remaining systematic deviation between the power law model and the measured data is quite small (<1%) and was modeled by a fifth-order polynomial. Based on this model, the extrapolated value of $f_{\rm zero}$ at 300 K is 101 kHz, which is lower than the value predicted by simulations (Section II). For ETF2, $f_{\rm zero}$ at 300 K is 292 kHz, which is significantly lower than the predicted value. The fitted value of $n = 1.6$, which is also lower than that obtained for ETF1. Since $f_{\rm zero}$ is about 3 times higher for ETF2 than for ETF1, these lower values may be caused by the preamplifier's phase-shift, which becomes increasingly significant at higher frequencies (Fig. 7).

For ETF1, the spread in $f_{\rm zero}$ (Fig. 13) is less than ±0.3% (3σ) over the industrial temperature range (−40 °C to 105 °C). This corresponds to a temperature-sensing inaccuracy of less than ±0.5 °C (3σ), which is comparable with the inaccuracy of batch-calibrated bipolar-transistor-based temperature sensors [4], [5]. This level of inaccuracy agrees well with the estimate based on (6) and on the estimated lithographic inaccuracy of the process. As expected, the spread in $f_{\rm zero}$ of ETF2 is about two times worse than that of ETF1 (Fig. 14), which further indicates that the observed spread may indeed be ascribed to lithographic inaccuracy. The converter's output jitter (into a 0.5 Hz bandwidth) corresponds to a noise level of about 0.04 °C (rms).

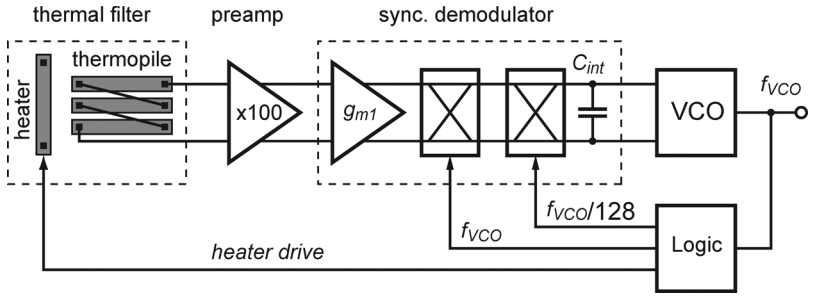

Fig. 8. Block diagram of a chopped electrothermal FLL.

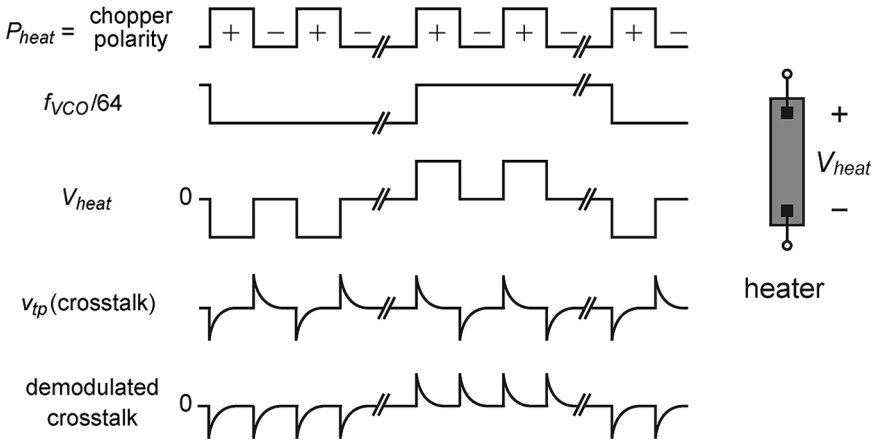

Fig. 9. Heater drive inversion (HDI): timing diagram.

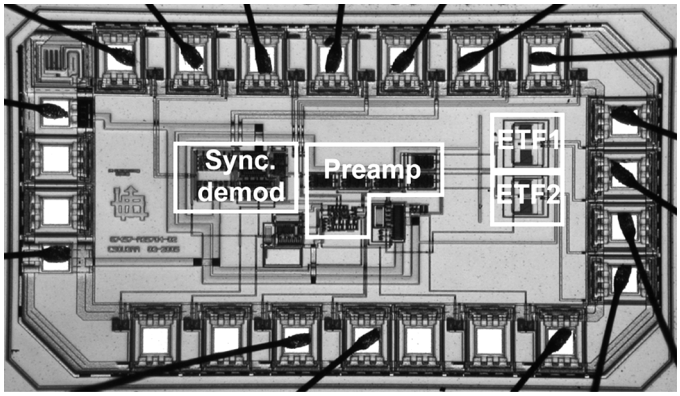

Fig. 10. Chip micrograph of the temperature-to-frequency converter front-end.

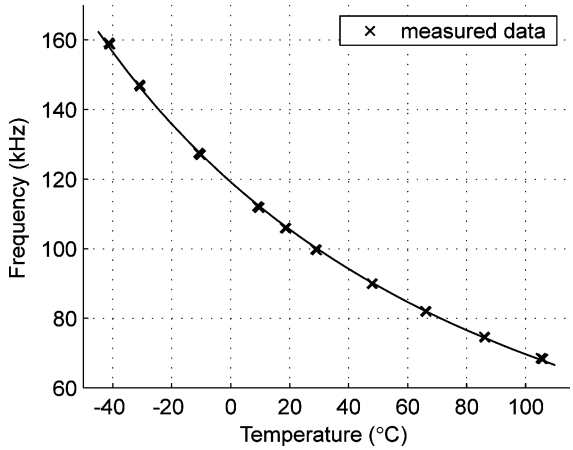

Fig. 11. Measured TFC characteristic (ETF1) and a $1/T^n$ fit.

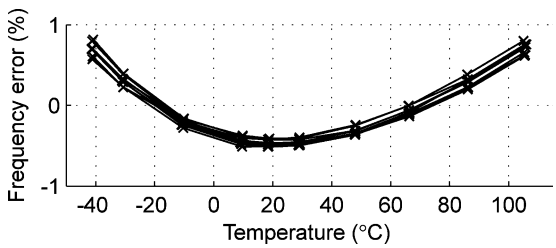

Fig. 12. Deviation of measured TFC characteristic (ETF1) from ideal $1/T^n$ fit.

VI. Conclusion

A temperature-to-frequency converter (TFC) based on the thermal diffusion constant of silicon has been described. It consists of a frequency-locked loop whose frequency is determined by the phase-shift of an electrothermal filter implemented in the substrate of a silicon chip. Since this phase-shift is a well-defined function of temperature, the output frequency of the TFC is also a well-defined function of temperature.

The performance of the TFC was evaluated by measurements on a test chip realized in a standard 0.7-μm CMOS process. Measurements on nine samples from one batch show that the output frequency of the TFC has an approximately $1/T^n$ dependence, where T is the absolute temperature in degrees Kelvin, and $n = 1.7$. The spread in the output frequency corresponds to a temperature-sensing inaccuracy of less than $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ). This level of inaccuracy was achieved *without* trimming, and is

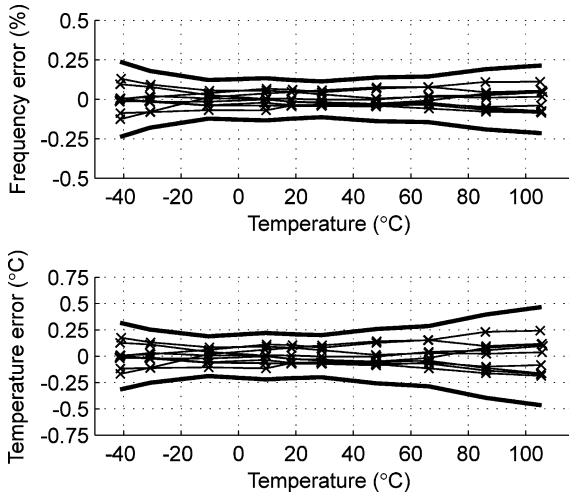

Fig. 13. Measured TFC spread (ETF1) with $\pm 3\sigma$ values (bold lines).

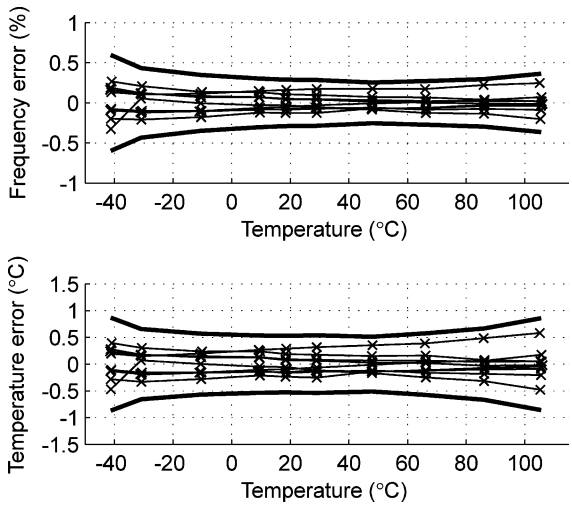

Fig. 14. Measured TFC spread (ETF2) with $\pm 3\sigma$ values (bold lines).

comparable with the intra-batch spread of conventional, bipolar-transistor-based, temperature sensors.

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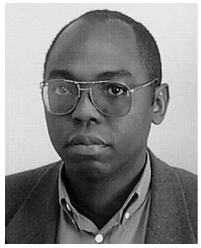

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