32.1 A CMOS Temperature-to-Digital Converter with an Inaccuracy of ±0.5°C (3σ) from –55 to 125°C

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This paper describes a CMOS temperature-to-digital converter (TDC) based on thermal diffusivity sensing, which is an interesting alternative to conventional band-gap temperature sensors because the thermal diffusivity of bulk silicon is insensitive to process spread. Compared to previous work [1, 2], this converter does not require off-chip analog components, operates over a wider temperature range and has a digital output. Furthermore, its output is a much more linear function of temperature. The TDC has an untrimmed device-to-device spread of ±0.5°C (3σ) over the military temperature range (–55 to 125°C).

The thermal diffusivity of silicon, D, is temperature dependent and can be approximated by $D \propto 1/T^n$ ($n \approx 1.8$) over the military temperature range [1]. D can be measured via the phase shift of an electrothermal filter (ETF), which consists of a heater and a thermopile realized in the substrate of a silicon chip. Figure 32.1.1 shows a CMOS ETF, in which the heater is an n^+-diffused resistor and the temperature sensor is a thermopile composed of 20 p^+-diffusion-aluminum thermocouples. Heat generated in the heater diffuses through the substrate, creating a temperature gradient that is sensed by the thermopile. Because of the chip's thermal inertia, this structure behaves like a low-pass filter whose phase shift is determined by D and by s, the spacing between the heater and the sensor. This phase shift is well defined because D is insensitive to process spread and s can be chosen large enough to minimize the effects of lithographic error.

When driven at a frequency f, the phase shift of an ETF, ϕ_{ETF}, is proportional to $s\sqrt{f/D}$. In the prior art [1, 2], this proportionality has been used as the basis of a temperature-to-frequency converter. Such a converter operates the ETF at a constant phase shift, so that its output frequency is proportional to $1/T^{1.8}$, being a rather non-linear function of temperature. Alternatively, the ETF can be driven at a constant frequency f_{drive}, so that its phase shift is proportional to $T^{0.9}$, which is a much more linear function of temperature (Fig. 32.1.2).

The temperature-dependent phase shift of an ETF can be digitized by a phase-domain delta-sigma modulator (PDΔΣM). The functional block diagram of a first-order single-bit PDΔΣM is shown in Fig. 32.1.3. The modulator's bitstream average represents the weighted average of two reference phase shifts (ϕ_0, ϕ_1) that best approximates the ETF's phase shift. The reference phase shifts are set to correspond to temperatures outside the military temperature range.

Figure 32.1.4 shows a block diagram of the PDΔΣM. The phase difference $\Delta\phi(=\phi_{ETF} - \phi_{ref})$ is obtained by multiplying the ETF's output with a reference signal, which has a phase shift ϕ_{ref} relative to f_{drive}. The multiplication is realized by a chopper at the output of a g_m-stage, and the resulting DC output current is integrated by a capacitor C_{int}.

The main challenge associated with interfacing an ETF is the low amplitude of its output signal. For a heater power P_{heat} of 1 milliwatt, the output will only be a few hundred microvolts. Since the thermopile also produces thermal noise, the noise bandwidth of the read-out circuitry has to be limited to a few Hertz, in order to obtain a temperature-sensing resolution below a tenth of a degree. In previous work, the bandwidth was limited with the help of a large off-chip integration capacitor (C_{int} = 1μF). In a PDΔΣM, however, the noise bandwidth is limited by the decimation filter, so that C_{int} can be scaled down to values that are compatible with CMOS integration. In this design, C_{int} was chosen to be 40 pF.

Due to the finite output impedance of the g_m-stage, the integrating capacitor C_{int} will suffer from leakage, which will give rise to dead-bands in the modulator's transfer characteristic. To ensure that these dead-bands are no wider than 0.05°C, the g_m-stage is implemented as a folded double-cascode OTA, whose simulated output impedance is in excess of 10GΩ over PVT. The OTA is preceded by a 3-stage preamplifier with an in-band gain of 30dB and a high-pass characteristic. The preamp reduces the thermopile-referred noise and the offset introduced by the g_m-stage. The preamplifier's high-pass characteristic is implemented with a DC servo-loop. To avoid introducing extra phase shift at f_{drive}, which would be indistinguishable from the ETF's phase shift, the associated cut-off frequency needs to be below 1kHz. In previous work, such a bandwidth required the use of an on-chip low-transconductance stage and a 470nF off-chip capacitor [1]. Here, a 10pF on-chip capacitor is used together with a small conductance (≤1nS) realized by the duty-cycle operation of long PMOS devices [3]. To further reduce offset, the entire front-end of the PDΔΣM is chopped twice during each conversion. As in [1, 2], heater drive inversion (HDI) is used to minimize errors due to capacitive cross-talk.

The ETF and the PDΔΣM were realized on a 2.3mm² 0.7μm CMOS chip, which is shown in Fig. 32.1.7. In order to effectively evaluate the performance of the new system, the geometry of the ETF was kept the same as that in [1], with s = 20μm. The ETF and the PDΔΣM each consume 2.5mW of power from a 5V supply.

The various timing signals required by the PDΔΣM were generated by an off-chip FPGA from a 16MHz crystal oscillator reference clock. The crystal's ±100ppm frequency inaccuracy corresponds to a temperature inaccuracy of ±0.05°C. The ETF is driven at f_{drive} = 85kHz, which represents a tradeoff between preamplifier bandwidth, ETF output amplitude and phase spread introduced by the finite (and variable) thickness of the die [4]. Reference phase ϕ_0 leads f_{drive} by 45 degrees, while ϕ_1 lags it by 45 degrees. The modulator's sampling frequency is 2.67kS/s. An off-chip 13b counter decimates the bitstream, resulting in a noise bandwidth of 0.33Hz and a quantization error of less than 0.05°C.

The measured phase shift as a function of temperature is shown in Fig. 32.1.5. The measured device-to-device spread is shown in Fig. 32.1.6 and is based on 16 devices from a single batch. The main source of spread is lithographic inaccuracy, corresponding to an untrimmed temperature inaccuracy of ±0.5°C (3σ) over the military temperature range; this accuracy is an improvement over [1], and is as good as state-of-the-art batch-calibrated temperature sensors based on bipolar transistors [5]. The dashed line in Fig. 32.1.6 shows the measured spread for low heater power (P_{heat} = 1mW); the slight degradation in spread is due to the decrease in SNR at the output of the ETF. At P_{heat} = 2.5mW, the TDC's temperature sensing resolution is $0.05°C_{rms}$ after decimation.

To examine the ETF's sensitivity to thermal interference (e.g. due to digital circuitry), a nearby resistor (120μm away) was driven with a 12mW pseudo-random heat signal derived from f_{drive}. The extra self-heating causes a die temperature increase of about 0.5°C, which is in line with the package's estimated thermal resistance. However, it does not decrease the TDC's resolution or increase the measured spread, demonstrating that thermal interference is effectively filtered by the thermal inertia of the die.

References:

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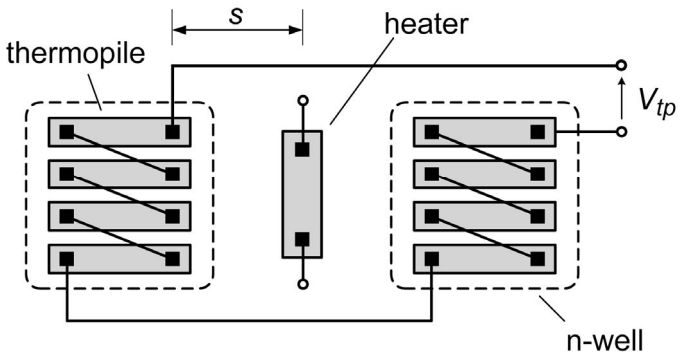

Figure 32.1.1: Schematic layout of an electrothermal filter (ETF) [1].

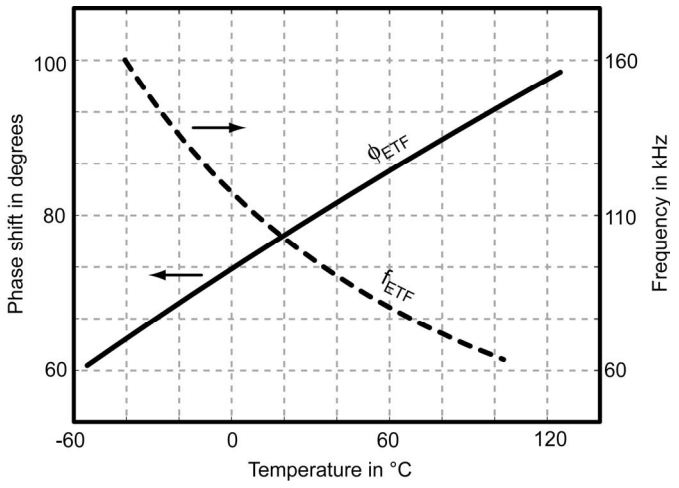

Figure 32.1.2: Simulated ETF output characteristics for both phase and frequency readout modes.

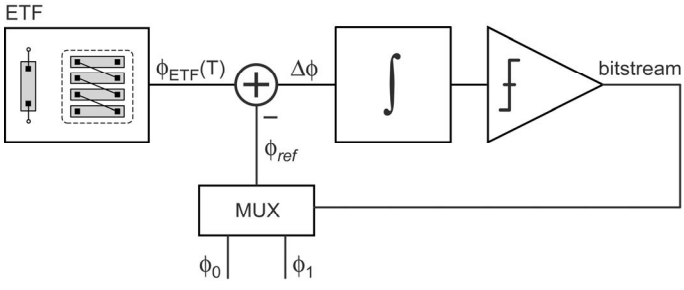

Figure 32.1.3: Block diagram of a phase-domain delta-sigma modulator (PDΔΣM), which digitizes the phase shift ϕ_{ETF} of an ETF.

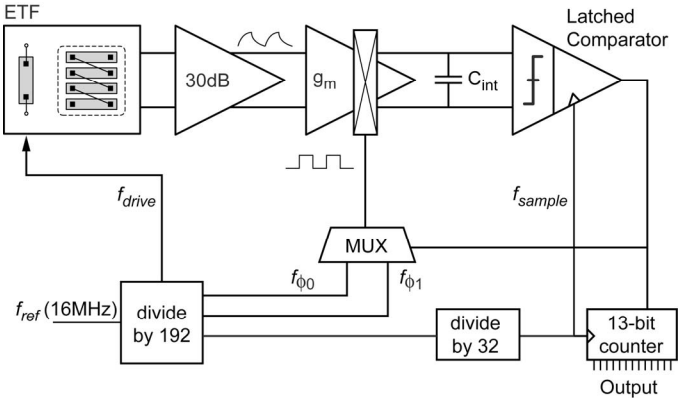

Figure 32.1.4: Block diagram of the PDΔΣM.

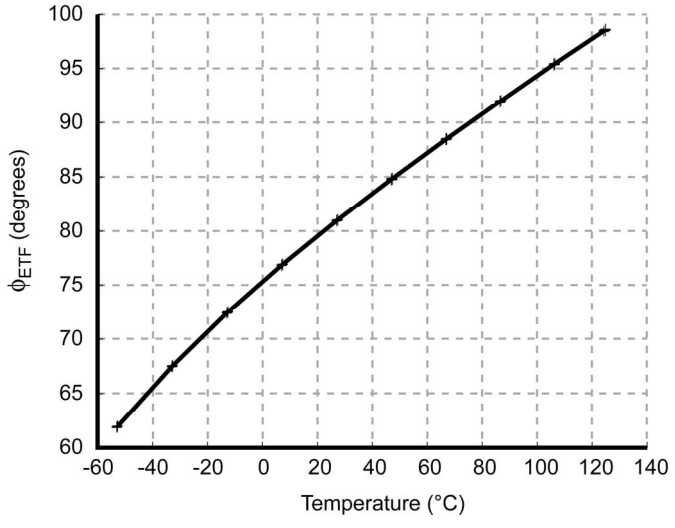

Figure 32.1.5: Measured ETF phase shift over temperature.

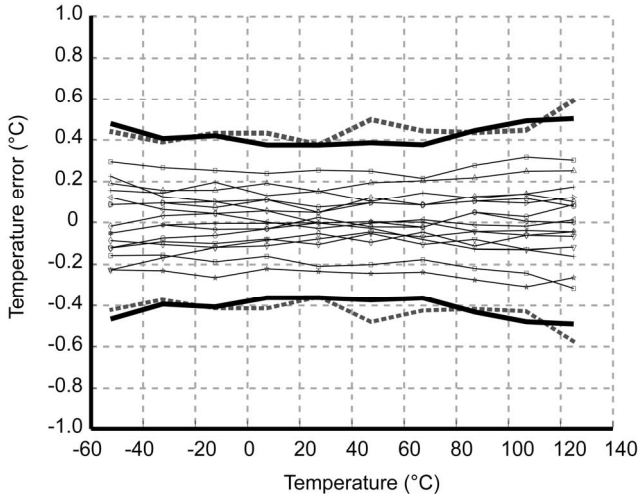

Figure 32.1.6: Measured temperature spread for 16 samples with P_{heat} = 2.5mW. Also shown are the ±3σ values (bold line: P_{heat} = 2.5mW, dashed line: P_{heat} = 1mW).

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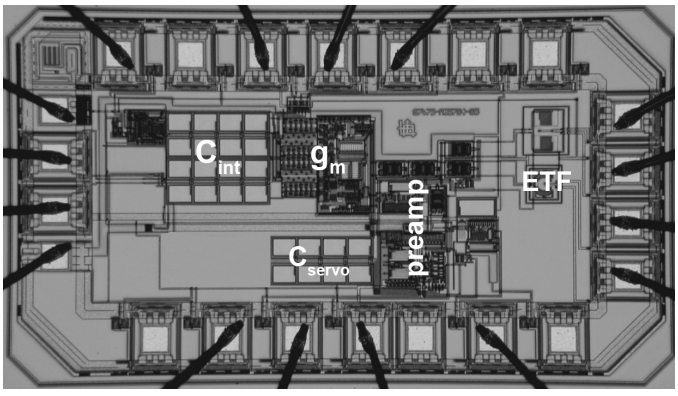

Figure 32.1.7: Chip micrograph of the ETF and the PDΔΣM.

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