A 6800-μm^2 Resistor-Based Temperature Sensor With $\pm$0.35 °C (3σ) Inaccuracy in 180-nm CMOS

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***Abstract*— This paper describes a compact resistor-based temperature sensor that has been realized in a 180-nm CMOS process. It occupies only 6800 μm^2, thanks to the use of a highly digital voltage-controlled oscillator (VCO)-based phase-domain sigma–delta modulator, whose loop filter consists of a compact digital counter. Despite its small size, the sensor achieves $\pm$0.35 °C (3σ) inaccuracy from −35 °C to 125 °C. Furthermore, it achieves 0.12 °C (1σ) resolution at 2.8 kSa/s, which is mainly limited by the time-domain quantization imposed by the counter.**

***Index Terms*— CMOS temperature sensor, phase-to-digital converter, thermal sensing, voltage-controlled oscillator (VCO)-based phase-domain sigma–delta modulator (PDΣΔM), Wien bridge (WB).**

I. Introduction

HEAT dissipation is a major issue in system-on-chips (SoCs) [1] since cooling techniques have failed to keep up with the growing energy density of modern processes. In consequence, SoCs heat up rapidly and may overheat if their power consumption is not throttled back. Overheating accelerates aging, degrades reliability, and may even cause a system failure. Therefore, modern SoCs usually incorporate thermal management systems, which monitor die temperature and throttle performance when needed either by reducing clock frequencies and/or supply voltages [2], [3].

The key specifications of such temperature sensors are speed, size, accuracy, and supply voltage insensitivity. Thermal transients have time constants in the order of a few milliseconds and, therefore, must be sampled at kSa/s rates. The heat distribution in an SoC will typically be non-uniform, featuring a number of so-called hot-spots whose intensity and location change dynamically as a function of workload. As a result, accurate thermal monitoring often requires the use of several tens of temperature sensors [4], and so each of them should be as small as possible. This makes it easier to include them in the layout of dense digital blocks and, therefore, easier to place near potential hot-spots. Moderate accuracy is required to reduce the safety margin between the measured and the desired performance throttling temperatures, and thus maximize performance. Finally, such sensors should be insensitive to supply voltage changes since performance throttling will change the latter significantly.

Most temperature sensors proposed for thermal management applications belong to one of the three types, i.e., bipolar junction transistor (BJT), gate-delay, and thermal-diffusivity-based temperature sensors. The most common are BJT-based temperature sensors [5]. In [6], a current-mode readout technique is used to realize a small (3800 μm^2) and moderately accurate (1.8 °C from −20 °C to 130 °C) n-p-n-based temperature sensor. In later work [7], the readout was modified to work with p-n-ps, which are more commonly available. Although BJT-based sensors can be quite accurate, their voltage headroom requirements do not scale with the technology. As a scaling-friendly alternative, sensors that exploit the temperature-dependent delay of CMOS logic gates have been proposed [8], [9]. Although they can be quite small, they are inherently sensitive to supply voltage variations and MOSFET aging. The third type of sensor exploits the temperature-dependent rate at which heat diffuses through silicon. Such thermal diffusivity (TD) sensors are as accurate as BJT-based sensors, can be quite compact (1650 μm^2 [10]), and scale well with the technology. However, they are comparatively power hungry [10]–[13].

Recently, temperature sensors based on silicided polysilicon resistors have been shown to be both stable, accurate, and energy efficient [14], [15]. The voltage insensitivity and large temperature coefficient (0.3%/°C) of this type of resistors make the resulting sensors well suited for use in thermal monitoring applications. However, only two resistor-based temperature sensor designs with areas less than 10 000 μm^2 have been reported so far [15], [16]. Of these, only [15] achieves good accuracy, but its output is a temperature-dependent frequency, and, therefore additional circuitry is required to generate a digital output.

This paper, an expanded version of [17], proposes ways of reducing the area of resistor-based temperature sensors while also maintaining their advantages: voltage insensitivity, accuracy, and energy efficiency. The result is a temperature sensor that achieves both small area (6800 μm^2) and good accuracy [$\pm$0.35 °C (3σ) after a two-point trim].

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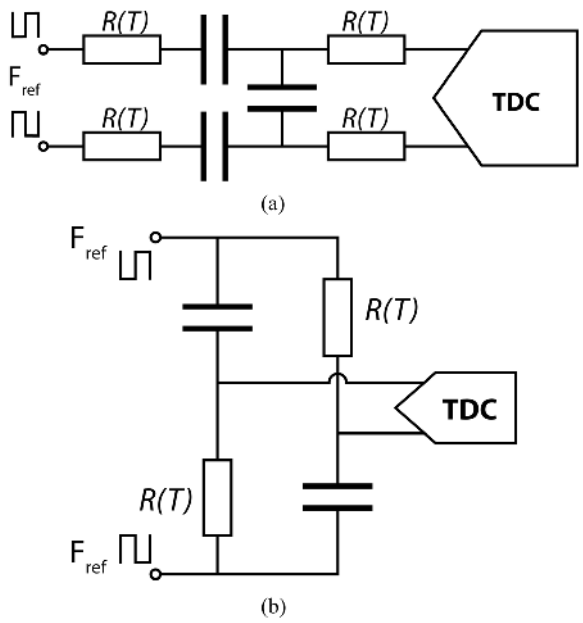

Fig. 1. (a) Differential WB. (b) PPF.

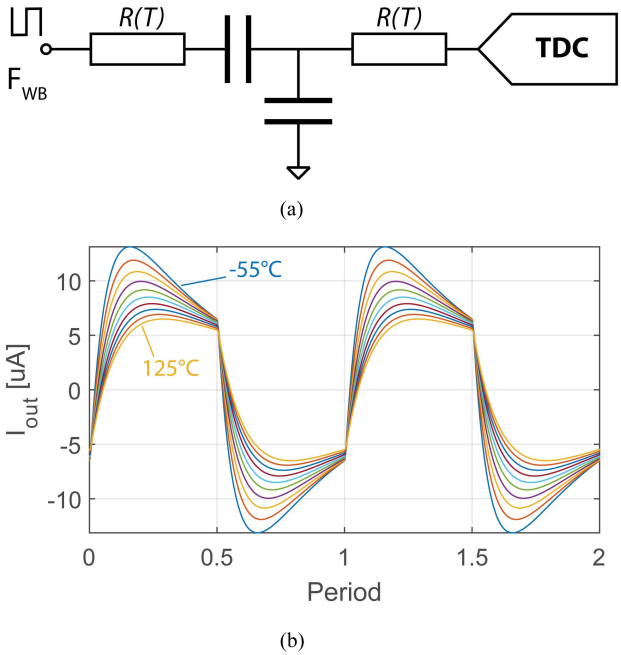

Fig. 2. (a) Single-ended WB. (b) Output waveform of a single-ended WB at different temperatures.

II. Resistor-Based Temperature Sensors

A. Sensor Topologies

There are two ways of using a temperature-dependent resistor $R(T)$ to generate a digital representation of temperature. The first involves the use of a Wheatstone bridge (WhB) to compare the value of $R(T)$ with that of a stable resistor, or to one with a different temperature dependence. The output of the bridge can then be digitized by an ADC [18]. The second involves the combination of $R(T)$ with a stable capacitor to realize a temperature-dependent RC filter, whose phase shift can then be digitized using a stable time reference [14]–[16].

On-chip resistors also suffer from process spread. This is particularly problematic in a WhB, which employs two different types of resistors, and, therefore, suffers from two different sources of spread [18]. Although on-chip capacitors also suffer from the spread, they are comparatively stable over temperature and so contribute much less temperature-sensing error. Furthermore, SoCs are usually clocked by sufficiently accurate time references. For example, for a Wien-bridge (WB) filter realized with 0.3%/K resistors, the 100-ppm frequency error of a typical low-cost crystal oscillator will only result in 0.025 °C temperature-sensing error.

B. Filter Choice

As shown in Fig. 1, two types of RC filters have been used in resistor-based temperature sensors: the WB [14] and the polyphase filter (PPF) [15]. Both combine first order low- and high-pass filters to achieve double the phase sensitivity of a first-order filter. However, a PPF requires fewer components than a WB filter. It also has slightly more phase sensitivity, at the expense of a slightly more non-linear resistance-to-phase characteristic. However, when driven by a rail-to-rail square wave, the output of a PPF will exceed the supply rails, which complicates the design of its readout circuitry. Although this is not the case for a WB, the resulting output voltage swing will still exceed the linear range of a simple differential pair. For this reason, WB sensors are usually read out in current-mode [Fig. 1(a)], by connecting the resistors in their output branches to a virtual ground [14] or to a current buffer [19].

In this work, a single-ended WB is used, which has the same number of components and occupies the same area as a PPF [Fig. 2(a)]. It is realized with silicided p-poly resistors ($R_{\mathrm{WB}} = 28\ k\Omega$) and MIM capacitors ($C_{\mathrm{WB}} = 1.84$ pF), resulting in a center frequency $F_{\mathrm{WB}} = 3$ MHz at room temperature. In the chosen 180-nm process, it occupies only 3700 μm^2. When driven by a 1.8-V square wave at F_{WB}, its output current is as shown in Fig. 2(b). It can be seen that both its shape (phase) and amplitude vary significantly over temperature.

III. System-Level Overview

Fig. 3 shows a simplified block diagram of the proposed system. It consists of 20 compact temperature sensors, together with shared bias current and phase reference generator, the latter being driven by an external frequency reference $F_{\mathrm{REF}}(= 75$ MHz). Each sensor consists of a single-ended WB, whose phase-shifted output current is digitized by a phase-domain sigma-delta modulator (PD$\Sigma\Delta$M) [12]. Instead of using an analog integrator based on large capacitors [12], the modulator's loop filter uses a compact discrete-time integrator based on a counter, which is driven by a current-controlled oscillator (CCO) [11]. In turn, the CCO is driven by a current buffer, whose low input impedance facilitates the current readout of the WB. To provide robustness against process spread, the center frequency of the CCO can be trimmed via a current DAC (IDAC). In Section IV, the design of each of these sub-blocks and their impact on sensor performance will be discussed in more detail.

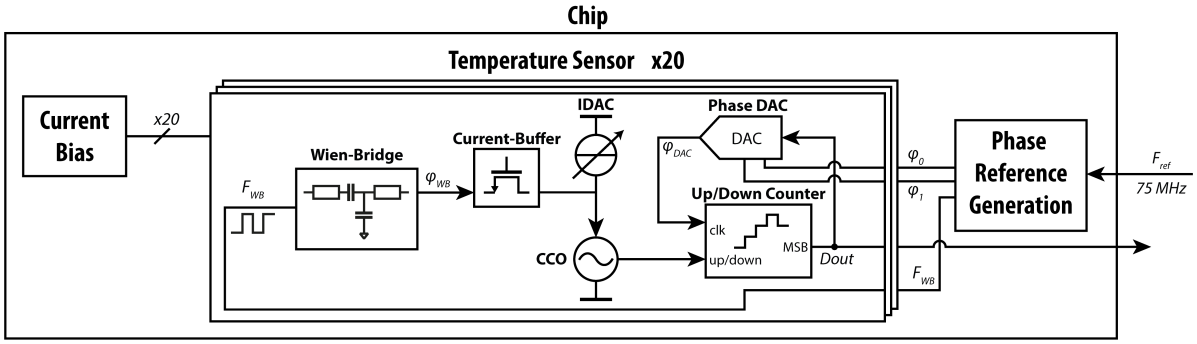

Fig. 3. System-level block diagram.

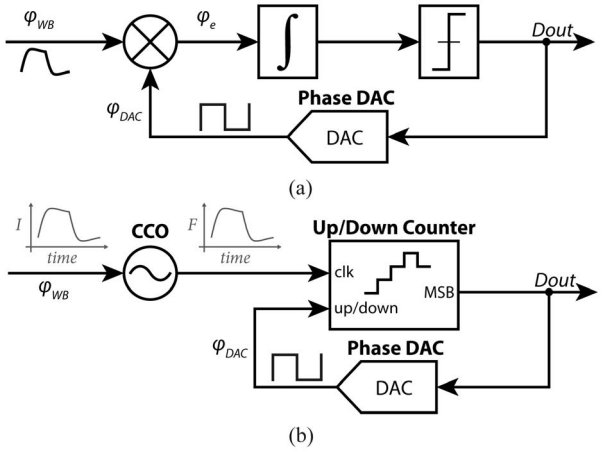

Fig. 4. (a) Block diagram of the phase-domain delta–sigma modulator [12]. (b) CCO-based phase-domain delta–sigma modulator [11].

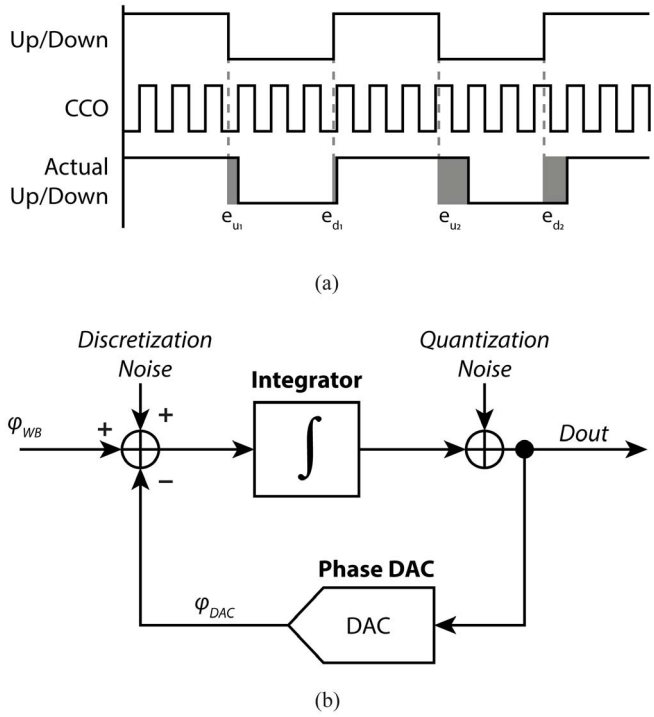

Fig. 5. (a) Timing diagram of the up/down and CCO signals. (b) Linear model of the voltage-controlled oscillator (VCO)-based phase-domain sigma–delta modulator.

IV. Phase-Domain Delta–Sigma Modulator

Fig. 4(a) shows a simplified block diagram of a PD$\Sigma\Delta$M [12]. An input phase ($\varphi_{\rm WB}$, at a frequency of $F_{\rm WB}$) is first multiplied by a feedback phase ($\varphi_{\rm DAC}$, also at a frequency of $F_{\rm WB}$). For sinusoidal signals, this results in a signal φ_e whose dc component is proportional to $\cos(\varphi_{\rm WB} - \varphi_{\rm DAC})$. For phase differences close to 90° P, $\cos(\varphi_{\rm WB} - \varphi_{\rm DAC} - 90°) \sim \varphi_{\rm WB} - \varphi_{\rm DAC}$ and so the demodulator effectively performs a phase-domain subtraction. In practice, the higher harmonics present in the WB output and the square wave of the phase DAC output also contribute to φ_e but the error is less than 5° P. The dc component of φ_e and the harmonics are integrated and then digitized by a 1-bit quantizer whose output is fed back to the phase DAC. This drives the multiplier's dc output to zero such that the average feedback phase $\varphi_{\rm DAC}$ is equal to $\varphi_{\rm WB} + 90°$P.

In this work, as shown in Fig. 4(b), the modulator's loop filter consists of a digital counter, which is driven by a CCO [11]. The latter converts the input signal from the current domain to the frequency domain, allowing the counter to be used as an integrator. By toggling the counter's up/down signal, the polarity of this integration can also be toggled, thus effectively multiplying the input signal with the up/down signal. The modulator's 1-bit quantizer can then be realized by simply sampling and evaluating the counter's MSB. The result is a highly digital PD$\Sigma\Delta$M [11], which can be easily scaled.

A. Counter Time-Discretization Noise

The downside of using a counter as an integrator is that it quantizes the phase of the CCO and, therefore, introduces time-domain discretization noise. Fig. 5(a) illustrates this: at the moment the up/down signal toggles, the CCO phase, and therefore the integrator's state, is quantized. In the example shown, the CCO goes through approximately 3.15 cycles in the first "up" counting period. However, the counter truncates this to 3 cycles, creating an error in the integrator state, and also creating an error at the start of the next "down" counting period, since it already starts at the truncated value. As shown in Fig. 5(b), this *discretization* noise can be modeled as an additive white-noise source at the input of the integrator [20] and, therefore, does not benefit from noise shaping.

Assuming that the transitions of the up/down signal are random with respect to the CCO phase, which is the case if the CCO frequency F_{CCO} is asynchronous with respect to the demodulating frequency F_{WB}, and/or if F_{CCO} is dithered by thermal noise, the counter's rounding error will have a uniform distribution. With this assumption, the total in-band phase noise (in radians) is given by [20]

$$\sigma_P = \sqrt{\frac{2}{3 \cdot OSR}} \cdot \frac{\pi F_{WB}}{F_{CCO,pp}} \quad (1)$$

where $F_{CCO,pp}$ is the peak-to-peak variation of F_{CCO} and over-sampling ratio (OSR) is the PD$\Sigma\Delta$M's OSR. It can be seen that the discretization noise can be minimized either by decreasing F_{WB}, increasing the modulator's OSR, or increasing the CCO's frequency swing. In this design, $F_{WB} = 3$ MHz, which in turn limits the modulator's sampling frequency to 3 MHz, since $F_s \leq F_{WB}$ in a PD$\Sigma\Delta$M. The OSR is then set by the signal bandwidth, which is defined by the desired conversion rate (3 kSa/s) and the choice of a simple sinc[1] decimation filter. On the other hand, increasing the CCO's frequency swing requires higher CCO frequencies, and hence higher power consumption. In this design, $F_{CCO,pp}$ is set to 600 MHz, which results in a resolution of 0.12 °C (rms). Although this is much worse than the mK-level resolution of the WB itself [19], it is good enough for thermal monitoring applications.

B. Up/Down Counter

Unlike an analog integrator, a counter does not clip. Instead, it wraps around. This corrupts the counter's state and, therefore, must be prevented. After one period of the sampling clock, the number of counts accumulated by the counter is given by [20]

$$C_\Delta = \frac{F_{CCO,pp}}{\pi F_{WB}} \cdot (\varphi_{WB} - \varphi_{DAC}). \quad (2)$$

In a PD$\Sigma\Delta$M, the counter's state oscillates around its mid-code; therefore, to prevent wrap-around, C_Δ should never exceed half the counter length.

From simulations, φ_{WB} varies by about 23° P over the targeted temperature range (−35 °C to 125 °C). With ±40% spread in *RC*, this results in a worst case phase difference $\varphi_{WB} - \varphi_{DAC}$ of about 40°. Given $F_{CCO,pp} = 600$ MHz and $F_{WB} = 3$ MHz, (2) indicates that the maximum value of C_Δ is 44. A 7-bit counter is thus required to prevent wrap-around.

To guarantee a 600 MHz (pp) frequency swing even in the presence of process variations, both the CCO and the counter are designed to operate up to 800 MHz over process, voltage and temperature (PVT). To achieve this, the counter is split up into two parts: a fine two-bit counter and a coarse 5-bit counter (Fig. 6) [13]. This reduces its power consumption since clock gating can be used to ensure that the coarse counter only operates at one quarter the frequency of the fine counter. The fine counter is a gray code counter, resulting in a faster and simpler implementation. To limit meta-stability issues to a single D flip-flop (D-FF) rather than to the entire counter, the up/down signal φ_{DAC} is re-clocked by F_{CCO}, before being applied to the counter.

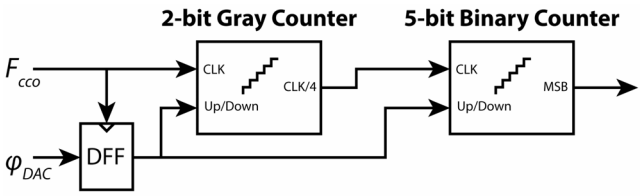

Fig. 6. 7-bit counter/integrator that splits into a 2-bit gray-code counter and a coarse 5-bit binary counter [13].

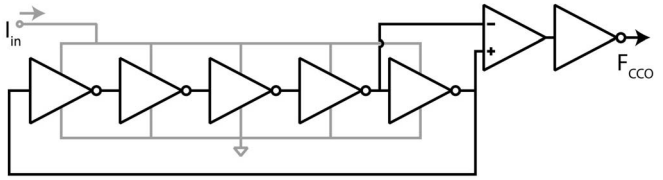

Fig. 7. 5-stage ring oscillator with a differential pair to level-shift the CCO swing to the full digital waveform.

The counter was synthesized using the normal digital design flow of the 180-nm CMOS process used. Operating at 800 MHz, it consumes 1 mW from a 1.8-V power supply, making it the most power-hungry sub-block of each sensor. However, in a more advanced process, its power consumption will scale dramatically, e.g., to about 130 μW in a 65-nm process.

C. CCO

The CCO consists of a five-stage chain of inverters, which converts the output current of the WB (30 μA pp) into the desired 600-MHz frequency swing. To mitigate the CCO center frequency's sensitivity to PVT, a 6-bit IDAC (∼30-MHz LSB) is used to trim the CCO's center frequency to ∼400 MHz at room temperature. Since this frequency is too high to be readily measured off-chip, the up/down counter is used as a divide-by-128 counter during trimming.

The inverter stages of the CCO do not output logic-compatible signals. Therefore, their outputs are amplified and level-shifted by a differential-pair (Fig. 7). After this, a simple inverter is enough to generate a rail-to-rail logic swing.

D. CCO Nonlinearity

As shown in Fig. 8, the CCO's current-to-frequency characteristic is quite non-linear. Since its output is multiplied by the square-wave output of the phase DAC, distortion components at odd harmonics of F_{WB} will fold back to baseband. In other words, any CCO non-linearity will cause errors in the error signal φ_e of the PD$\Sigma\Delta$M. Although the CCO frequency swing could be limited to improve linearity, this would increase the discretization noise. Fortunately, any systematic errors will be accounted for during the sensor's calibration, while any spread can be mitigated by trimming.

Monte-Carlo simulations results are plotted in Fig. 9 and show the additional phase shift resulting from CCO non-linearity. Although this is significant (ranging from 0.2° P to 0.5° P), its spread (mainly offset) is relatively small and

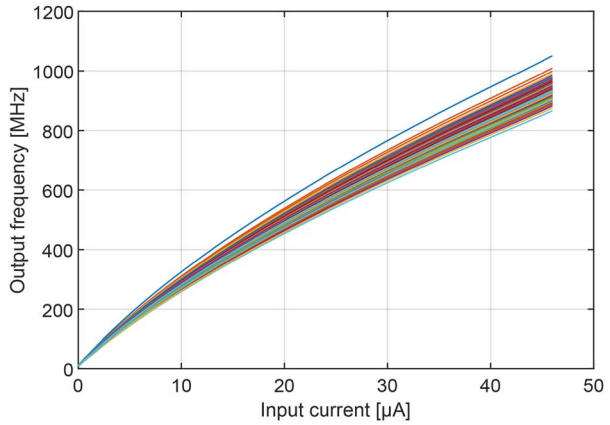

Fig. 8. Monte-Carlo (process + mismatch) simulation of the CCO current-to-frequency transfer.

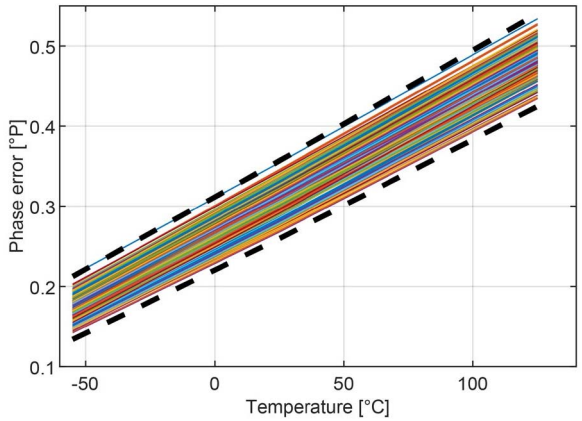

Fig. 9. Simulated additional phase shift due to the CCO non-linearity at −55 °C, 25 °C, and 125 °C (Monte-Carlo process + mismatch). Dashed line: 3σ values.

can be reduced to less than 80 mK (3σ) after a one-point trim.

Variations in the WB's output current swing will also vary the CCO's effective non-linearity, which, in turn, will cause variations in the detected WB phase. This may be due to power supply variations and/or the spread (±20%) of the WB resistors. The former will result in a finite power supply sensitivity, which is simulated to be 5.3 °C/V, close to the measured supply sensitivity of 4.6 °C/V. The latter will cause variations in the measured phase (Fig. 10) and therefore increase inaccuracy. This can only be somewhat mitigated by trimming: to 1.2 °C (3σ) after a one-point trim, and to 0.13 °C (3σ) after a two-point trim.

E. Current Buffer

As seen from its supply terminals, the impedance of the CCO is quite significant compared to that of the WB resistors. Therefore, to avoid altering its phase response, a current buffer is inserted between the WB and the CCO. As shown in Fig. 11, the current buffer consists of a common-gate amplifier (M1), with an input impedance ($1/\text{gm} \sim 600\ \Omega$) $\ll R_{\text{WB}}$ at F_{WB}, and a folded-cascode output that drives the CCO. Since they are both small (for speed and area) and the CCO input has a large

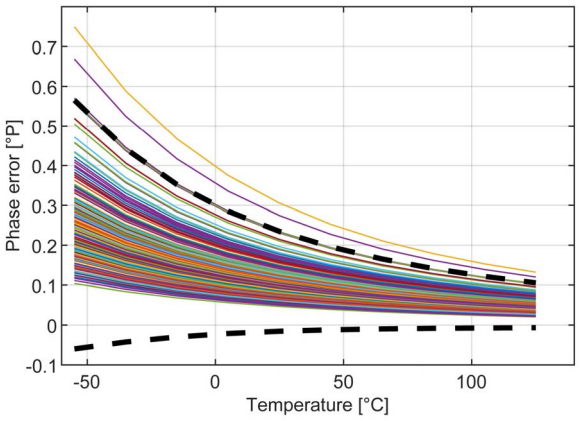

Fig. 10. Simulated Monte-Carlo (process + mismatch) spread due to amplitude variations in the WB output current.

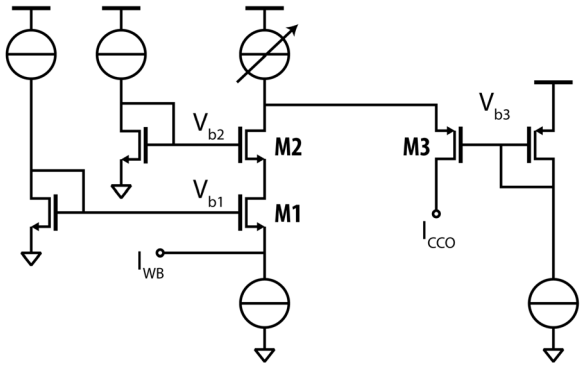

Fig. 11. Cascodes in the current-buffer reduce the input impedance as seen from the WB side.

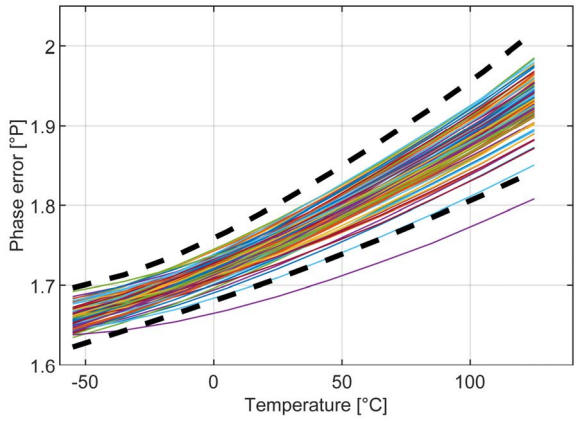

Fig. 12. Simulated Monte-Carlo (process + mismatch) spread due to current buffer and bias spread.

voltage swing, two cascodes (M2, M3) are used to prevent the voltage swing across the CCO from entering the WB. The required bias voltages are generated by diode-connected MOSFETs, each of which is biased with a nominal 5.6 μA.

Fig. 12 shows the simulated phase shift spread due to the spread of the current buffer and its bias current. Once more, there is a relatively large average shift (∼1.8° P) and a non-linear temperature dependence, both of which will be corrected during the sensor's calibration. Simulations show that the

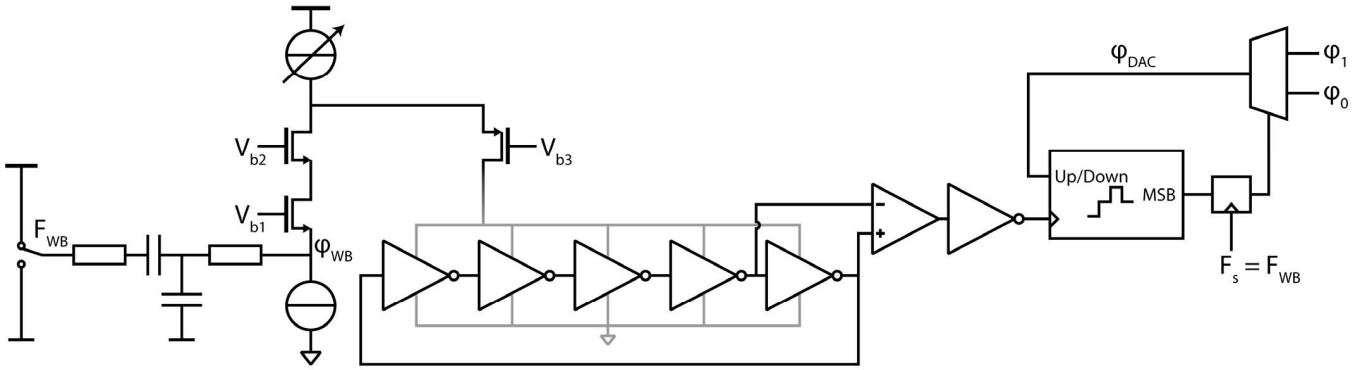

Fig. 13. Complete sensor overview.

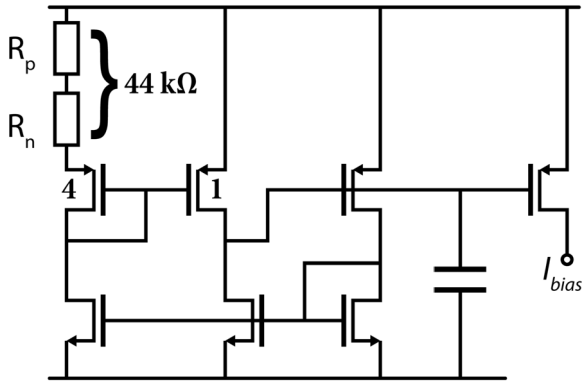

Fig. 14. Circuit diagram of the bias source.

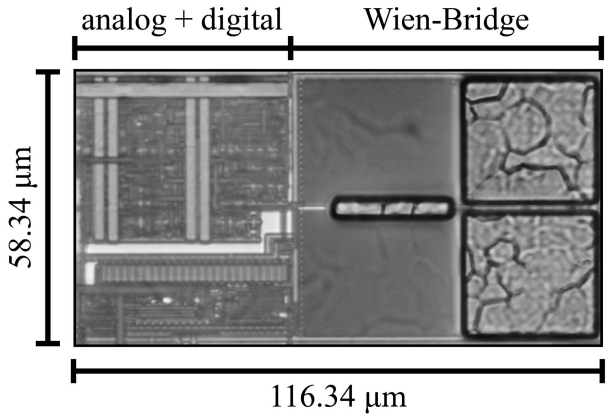

Fig. 15. Chip photograph.

resulting temperature error is less than 0.6 °C after a one-point and less than 0.1 °C after a two-point trim.

F. Shared Bias and Phase Reference Generation

Fig. 13 shows the complete system, in which the WB is driven by a square-wave signal at F_{WB}, which then generates an output current with a phase shift φ_{WB}. This is then fed to the current buffer and used to drive the CCO, which, in turn, drives the PD$\Sigma\Delta$M. A phase generator provides the required reference signals ($F_{\mathrm{WB}} = 0°$, $\varphi_0 = 90°\ \mathrm{P} - 20°\ \mathrm{P}$, and $\varphi_1 = 90°\ \mathrm{P} + 20°\ \mathrm{P}$).

The phase reference generator is driven by an external 75-MHz clock. It consists of a programmable divide-by-2N counter, whose output is a square wave with a frequency of F_{WB} and a 50% duty cycle. This is then used to drive the WB, as well as a programmable delay chain, which generates the phase references used by the phase DAC. As shown in Fig. 3, the phase generator is shared by all 20 temperature sensors on the same chip. It occupies 1200 μm^2 and dissipates less than 0.1 mW (simulated). It should be noted that a non-programmable generator would only occupy 430 μm^2.

The bias current generator (Fig. 14) operates by forcing a proportional to absolute temperature voltage across a resistor. A composite resistor, made by combining two resistors with opposite temperature coefficients, ensures that the resulting current is relatively flat over temperature. This current is then mirrored out to all 20 sensors. The residual curvature is less than 10%, which means that a single trim is sufficient to ensure that the CCO operates properly over the military temperature range. The bias current generator dissipates about 33 μW and occupies 2500 μm^2.

V. Measurements

The system was realized in a standard 180-nm CMOS technology (Fig. 15). Each chip contains 20 temperature sensors, which each occupies 6800 μm^2, as well as a shared bias current and a phase reference generator. The system operates from a 1.8-V supply voltage and dissipates 1.6 mW (60% is consumed by the counter, 39% by the current buffer and CCO, and 1% by the WB).

Due to the finite input impedance of the current buffer, and the spread and parasitic capacitances of the WB resistors, the average center frequency of the implemented WB filters is a bit lower than 3 MHz. To accommodate this, all the sensors were driven at $F_{\mathrm{WB}} \approx 2.9$ MHz(= 75 MHz/2·13). A fast Fourier transform (FFT) of the PD$\Sigma\Delta$M's bitstream output (Fig. 16) confirms that the sensor's noise floor is indeed dominated by the counter's discretization noise. After decimation by an off-chip 1024-tap sinc^1 filter, the sensor achieves a resolution of 0.12 °C (1σ) at a conversion rate of 2.8 kSa/s, which is in good agreement with the discretization noise levels predicted by (2).

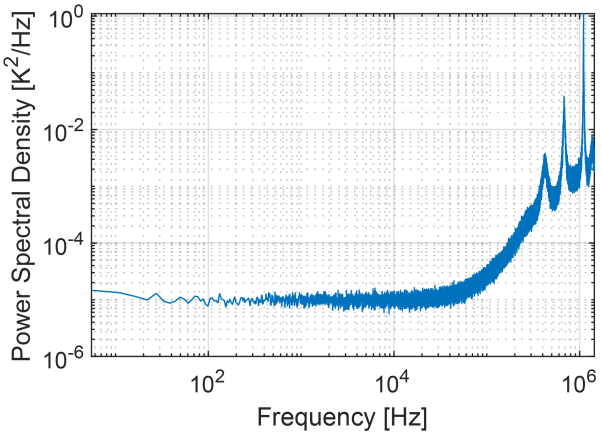

Fig. 16. PSD of 2^{19} bit-stream samples (with the mean value removed to better observe LF noise), averaged 100×.

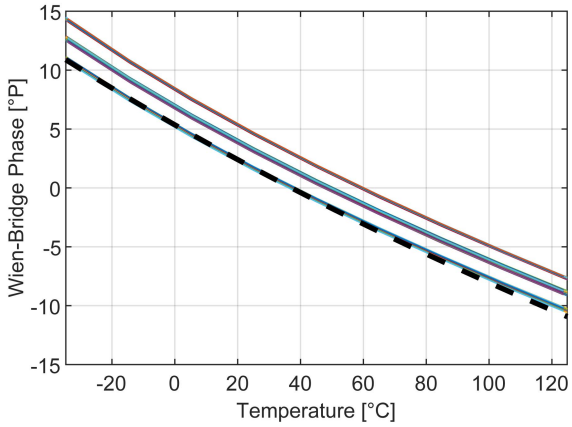

Fig. 17. Measured phase of 160 samples from 8 chips compared to the simulated phase (dashed line).

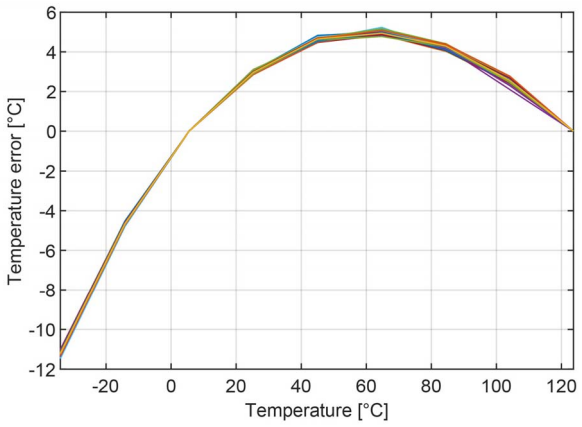

Fig. 18. Temperature error of 160 samples from 8 chips after two-point trim but before systematic non-linearity correction.

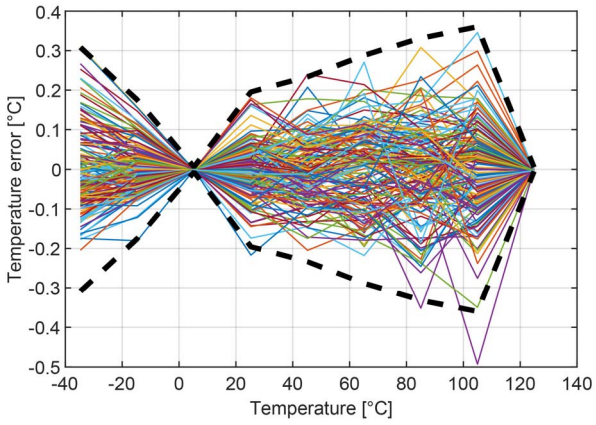

Fig. 19. Measured inaccuracy of 160 samples from 8 chips after a two-point temperature trim. Dashed line: 3σ error.

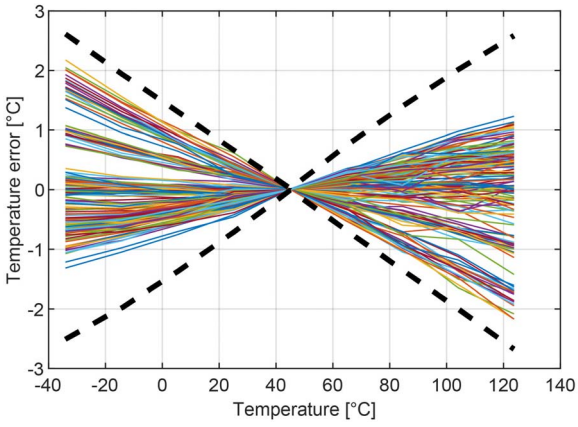

Fig. 20. Measured inaccuracy of 160 samples from 8 chips after a one-point temperature trim. Dashed line: 3σ error.

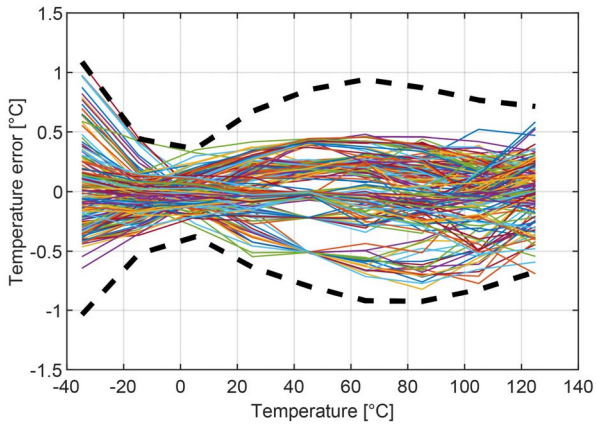

Fig. 21. Measured inaccuracy of 160 samples from 8 chips after a correlated one-point temperature trim. Dashed line: 3σ error.

The sensor's output over temperature is shown in Fig. 17 (160 samples from 8 chips). After a two-point trim (at 5 °C and 125 °C), the remaining error is dominated by a systematic non-linearity (Fig. 18). This can be removed by a fixed third order polynomial [19] (Fig. 19), resulting in an inaccuracy of $\pm$0.35 °C (3σ) from $-$35 °C to 125 °C.

After a 1-point offset trim, the sensor achieves an inaccuracy of $\pm$2.7 °C (3σ) (Fig. 20). This can be improved to $\pm$1.2 °C (Fig. 21) by applying a correlated one-point trim [14]. This trim relies on the correlation of offset and gain errors of individual sensors with respect to their average master curve (Fig. 22), and so the gain error can be estimated from the offset

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

Publication	*This Work*	*U. Sonmez* [10]	*S. Pan* [14]	*W. Choi* [15]	*Y-C Hsu* [21]	*M. Eberlein* [6]
Year	2018	2016	2018	2018	2017	2016
Type	Resistor	TD	Resistor	Resistor	PNP	NPN
Technology	180nm	40nm	180nm	65nm	28nm	28nm
Area (μm²)	6800[1]	1650[1]	720000[1]	7000[1]	9461	3800
Inaccuracy (3σ, °C)	-	1.4	-	-	0.87	1.8
Inaccuracy, 1-pt trim (3σ, °C)	-	0.75	0.2	2.47	-	-
Inaccuracy, 2-pt trim (3σ, °C)	0.35	-	0.03	0.12	-	-
Temperature Range (°C)	-35 to 125	-40 to 125	-40 to 85	-40 to 85	0 to 125	-20 to 130
Resolution (°C)	0.12	0.36	0.00041	0.0025	0.15	0.5
Speed (kSa/s)	3	1	0.2	1	0.12	31.25
Supply Voltage (V)	1.8	0.9-1.2	1.6-2.0	0.85-1.05	1.8	1.1-2.0
Supply Sensitivity (°C/V)	4.6	2.8	0.17	0.5	-	0.1[2]
Power (mW)	1.6[1]	2.5[1]	0.16[1]	0.068[1]	0.01875	0.0176

[1] Additional circuitry required (e.g. bias current and phase reference generators (this work), decimation filters (this work, [10, 13] or frequency-to-digital converters [14]). [2] Simulated, measured <0.5LSB~0.33°C/V.

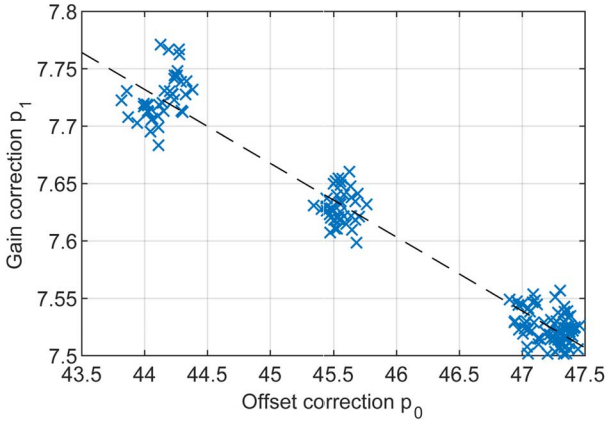

Fig. 22. Correlation between offset correction p_0 and gain correction p_1.

at 45 °C. Simulations show that this correlation is mainly due to the phase errors caused by CCO non-linearity. In Table I, the sensor's performance is compared to other state-of-the-art temperature sensors. The area and power of the bias and phase generators are not included, since these are both negligible compared to that of the 20 sensors.

As stated before, the CCO center frequency will spread over PVT and so must be trimmed to about 400 MHz. Since the intra-batch CCO spread is small and the same bias current generator is used, the same trim code can be used for all the CCOs on one die. This means that in practice, only one CCO (of the 20) needs to be trimmed, which considerably reduces the required effort.

VI. CONCLUSION

A compact and accurate resistor-based temperature sensor has been proposed. Compared to other resistor-based temperature sensors aimed at thermal management, this design achieves competitive area and accuracy despite being realized in a mature 180-nm process. Its low area is mainly due to the use of a highly digital CCO-based ADC. This design scales well with technology and its performance is expected to improve when ported to more advanced processes.

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